

COMPAL CONFIDENTIAL

MODEL NAME : Warlock TGL

PCB NO : DA6002E0000

PCB 2X2 LA-L241P REV0 M/B 1 S

TGL-U+MEC1515  
(UMA) - Realtek Codec  
2021-04-07  
REV : 1.0 (A00)

TGL CPU QS

UC1  
SA0000DRS1L  
QS\_I3@  
S IC A31 FH8069004531502 QVBG B1 3G S

UC1  
SA0000DRR1L  
QS\_I5@  
S IC A31 FH8069004530601 QVBD B1 2.4G S

UC1  
SA0000DRG1L  
QS\_I7@  
S IC A31 FH8069004529905 QVBA B1 2.8G S

TGL CPU Base-U

UC1  
SA0000DXG2L  
PENTIUM@  
S IC A31 FH8069004531802 QVBK B1 2G S

UC1  
SA0000DXH2L  
CELERON@  
S IC A31 FH8069004531901 QVBS B1 1.8G S

TGL CPU R3

UC1  
SA0000DTV2L  
R3\_I3@  
S IC FH8069004531602 SRK08 B1 3G A31 !


UC1  
SA0000E4U3L  
R3\_I34C@  
S IC FH8069004531606 SRK8S B1 2G A31 !

UC1  
SA0000DTU2L  
R3\_I5@  
S IC FH8069004531301 SRK05 B1 2.4G A31 !

UC1  
SA0000DTT2L  
R3\_I7@  
S IC FH8069004530104 SRK02 B1 2.8G A31 !

@ : Un-pop Component  
UMA@ : not Support external Graphic card  
N3@/V3@ : Inspiron/Vostro  
MSFT@/NMSFT@ : MSFT SKU / Normal SKU  
G3@ : Support G3 sharing SPI topology  
CNV@ : Support CNVi function  
S5LID@/LID@ : Support S5 LID power up Function/Normal LID close  
ES\_I3@/ES\_I5A@/ES\_I5B@/QS\_I7@ : TGL-U QS Sample  
STG@ : C10\_gate control VCCSTG  
I2CTCH@/USBTCH@ : Touch Screen support I2C signal / USB signal  
BASE@/PREM@ : Pentium,Celeron/i3,i5,i7  
I2CPAD@/PS2PAD@ : EC use I2C touch PAD signal(or PS2)  
JP@/JUMP@/PJP@ : JUMP  
100@/1000@ : 10/100 LAN / Giga-LAN  
PRO@/ICPRO@ : only LCDVDD protection/Hinge up protection Support  
EMI@/ESD@/RF@ : EMI, ESD and RF Component  
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component  
CMC@ : XDP Component  
CONN@ : Connector Component  
KBBL@ : KB Backlight  
TPM@/NTPM@ : HW TPM/SW TPM  
750\_CTPM@ : 750 and china TPM  
CTPM@/ST\_CTPM@ : China TPM/ST China TPM  
FFS@ : Free Fall Sensor  
TYPEC@/NTYPEC@ : Support TypeC/non-TypeC  
TYPEC@EMI@/TYPEC@ESD@ : EMI, ESD ,TypeC Component  
LBIST@/LBIST@RF@ : LBIST for LCD monitor  
TP@/CMC@TP@ : Test Point/XDP Test Point  
DISPCB@/UMAPCB@ : PCB MB

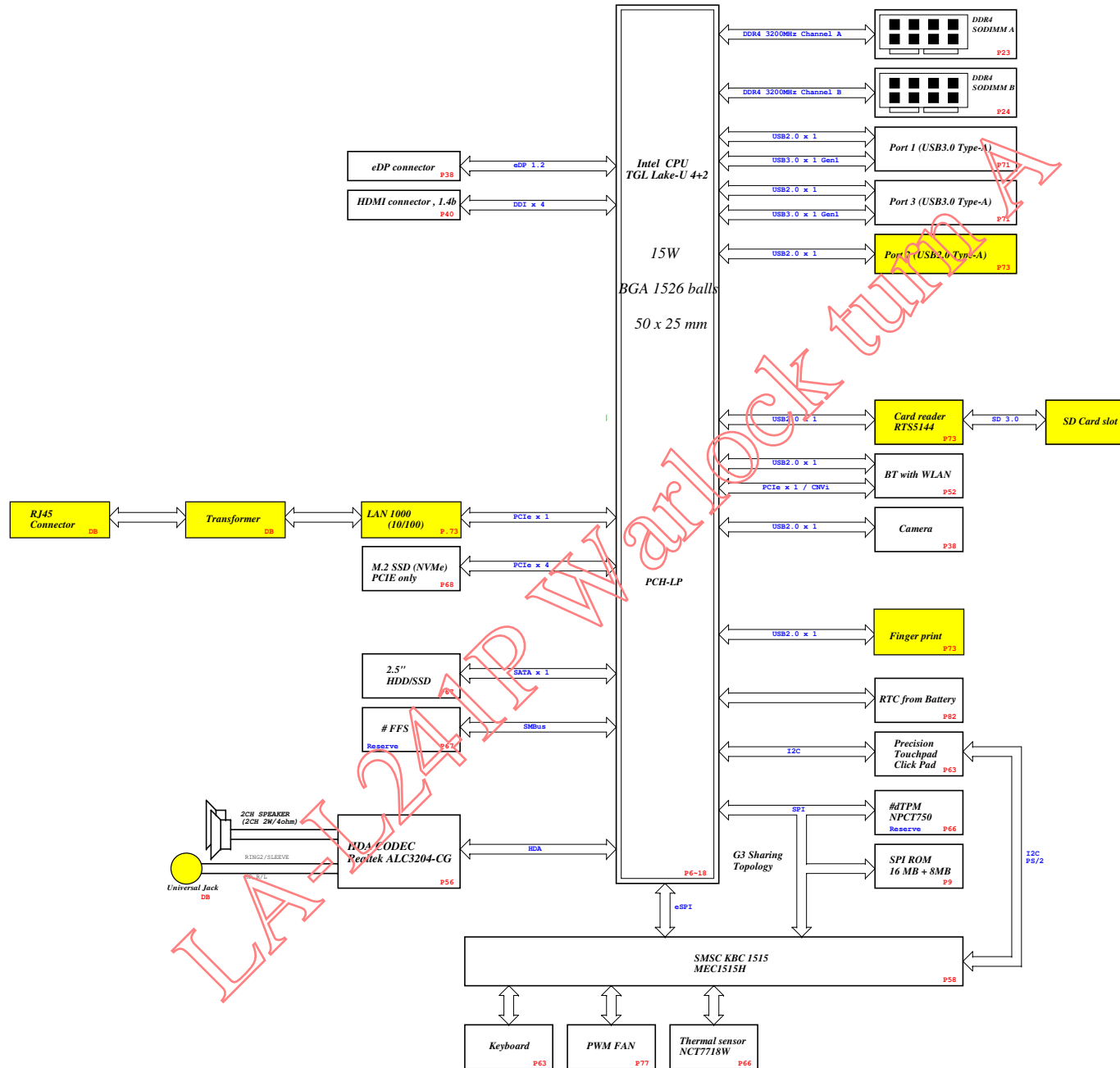
Layout Dell logo



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PWB: 9HTP8

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# Block Diagram



POWER STATES

Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
State							
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	---	---	---	---	---	---	---

USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 Port2
3	USB2.0 port3, IO/B
4	NC
5	Finger printer
6	CCD
7	Card reader , IO/B
8	NC
9	Reserved
10	BT

Board ID & Model ID Table

Bullseye TGL			
NBDR	SKU	Model-ID (RE4 PD-100K)	Board-ID (RE2 PD-100K)
	UMA	RE3 PU-10K	RE1 PU-10K -EVT RE1 PU-17.8K -DVT1 RE1 PU-27.0K -Reserve RE1 PU-37.4K -DVT2 RE1 PU-49.9K -Reserve RE1 PU-64.9K -Pilot RE1 PU-82.5K -Reserve
	DSC - N175-G3	RE3 PU-17.8K	

Voltage Rails

Power Plane	Description	S0	S3	S4/S5	G3
+19V_ADPIIN	Adapter power supply	N/A	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for System	N/A	N/A	N/A	N/A
+RTC_SOC	RTC power	ON	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*	OFF
+5VALW	System +5V always on power rail	ON	ON	ON*	OFF
+3VALW	System +3V always on power rail	ON	ON	ON*	OFF
+1.8V_PRIM	System +1.8V always on power rail	ON	ON	ON*	OFF
+1.0V_PRIM	System +1.0V always on power rail	ON	ON	ON*	OFF
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	ON	ON	OFF
+VCCST	+1.05 VCCST power rail	ON	ON	ON	OFF
+VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF	OFF
VCCPLL	+1.05 VCCPLL power rail	ON	ON	ON	OFF
+VCC_IN	Core voltage for CPU	ON	OFF	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	OFF
+3VALW_DSW	+19VB to DSW power rail for suspend power	ON	ON	ON	OFF
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	ON*	OFF
+5VS	System +5VS power rail	ON	OFF	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF	OFF
+1.35V_MEM GFX	+1.35V power rail for GPU	ON	OFF	OFF	OFF
+3VGS	+3V power rail for GPU	ON	OFF	OFF	OFF
+1.8VGS	+1.8V power rail for GPU	ON	OFF	OFF	OFF
+0.95VSDGPU	+0.95V power rail for GPU	ON	OFF	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF

RE: ICL N3V3 MLK High Power Consumption on VCCIN\_AUX Under S3/S5

Wu, Eddie <eddie.wu@intel.com>

发件日期: 2019/5/6 (周二) 下午 09:41

收件人: Chen, Deval (TFB); Chen, Johany (TFB); Huang, Henry (TFB); Chang, Ivy Si; Lan, Joe (TFB); Lai, Carol (TFB); Erenzy,Luo@del.com

副本: Chen, AlexCL (TFB); Chang, Gary; ; Hase, Jimmy

Hi David,  
VCCIN\_AUX only down to 0V while SLP\_S0# is asserted.  
On S3 mode, it only can down to 1.1V. Thanks.

Best Regards,  
Eddie Wu +886-2-66221110

10.12.4 Power States

Table 207. System with M3 State Supported

Rails	SKUs	S0/M0 3	C102	S0ix/M-off*	S3/M3	S3/M-off	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G3+
VCCRTC	All	ON	ON	ON	ON	ON	ON	ON	ON	ON
VCCDSW_3P3	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
V5.0A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_3P3	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_1P8	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCC_VNNEXT_1 P05	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCC_V1P0SEXT_1P05	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V3.3M5	All	ON	ON	OFF	ON <sup>10</sup>	OFF	ON <sup>10</sup>	OFF	OFF	No Power
V1.8M5	All	ON	ON	OFF	ON <sup>10</sup>	OFF	ON <sup>10</sup>	OFF	OFF	No Power
VDDQ	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
V2.5U (VPP)	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
VCCST	All	ON	ON	ON	ON <sup>13</sup>	ON <sup>13</sup>	OFF <sup>6</sup>	OFF <sup>6</sup>	OFF	No Power
VCCSTG	All	ON	OFF <sup>2</sup>	OFF	OFF	OFF	OFF	OFF	OFF	No Power
V3.3S	All	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	No Power
VCCIN	All	ON	ON	ON <sup>11</sup>	OFF	OFF	OFF	OFF	OFF	No Power
VCCIN_AUX	All	ON	ON	ON <sup>11</sup>	OFF <sup>14</sup>	OFF <sup>14</sup>	OFF <sup>14</sup>	OFF <sup>14</sup>	OFF	No Power

Note : VCCIN\_AUX only down to 0V while SLP\_S0# is asserted. On S4 mode, it only can down to 1.1V.

Board ID & Model ID Table

Bullseye TGL			
NBDR	SKU	Model-ID (RE4 PD-100K)	Board-ID (RE2 PD-100K)
	UMA	RE3 PU-10K	RE1 PU-10K -EVT RE1 PU-17.8K -DVT1 RE1 PU-27.0K -Reserve RE1 PU-37.4K -DVT2 RE1 PU-49.9K -Reserve RE1 PU-64.9K -Pilot RE1 PU-82.5K -Reserve
	DSC - N175-G3	RE3 PU-17.8K	

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1	PCIE-1		USB3.0 (MB)(Type-A)
USB3.0-2	PCIE-2		USB3.0 (MB)(Type-A)
USB3.0-3	PCIE-3		NC
USB3.0-4	PCIE-4		NC
	PCIE-5		PCIE SSD
	PCIE-6		PCIE SSD
	PCIE-7		PCIE SSD
	PCIE-8		PCIE SSD
	PCIE-9		LOM
	PCIE-10		WLAN
	PCIE-11	SATA-0	SATA HDD
	PCIE-12	SATA-1	NC
	PCIE4 - 0		NC
	PCIE4 - 1		NC
	PCIE4 - 2		NC
	PCIE4 - 3		NC

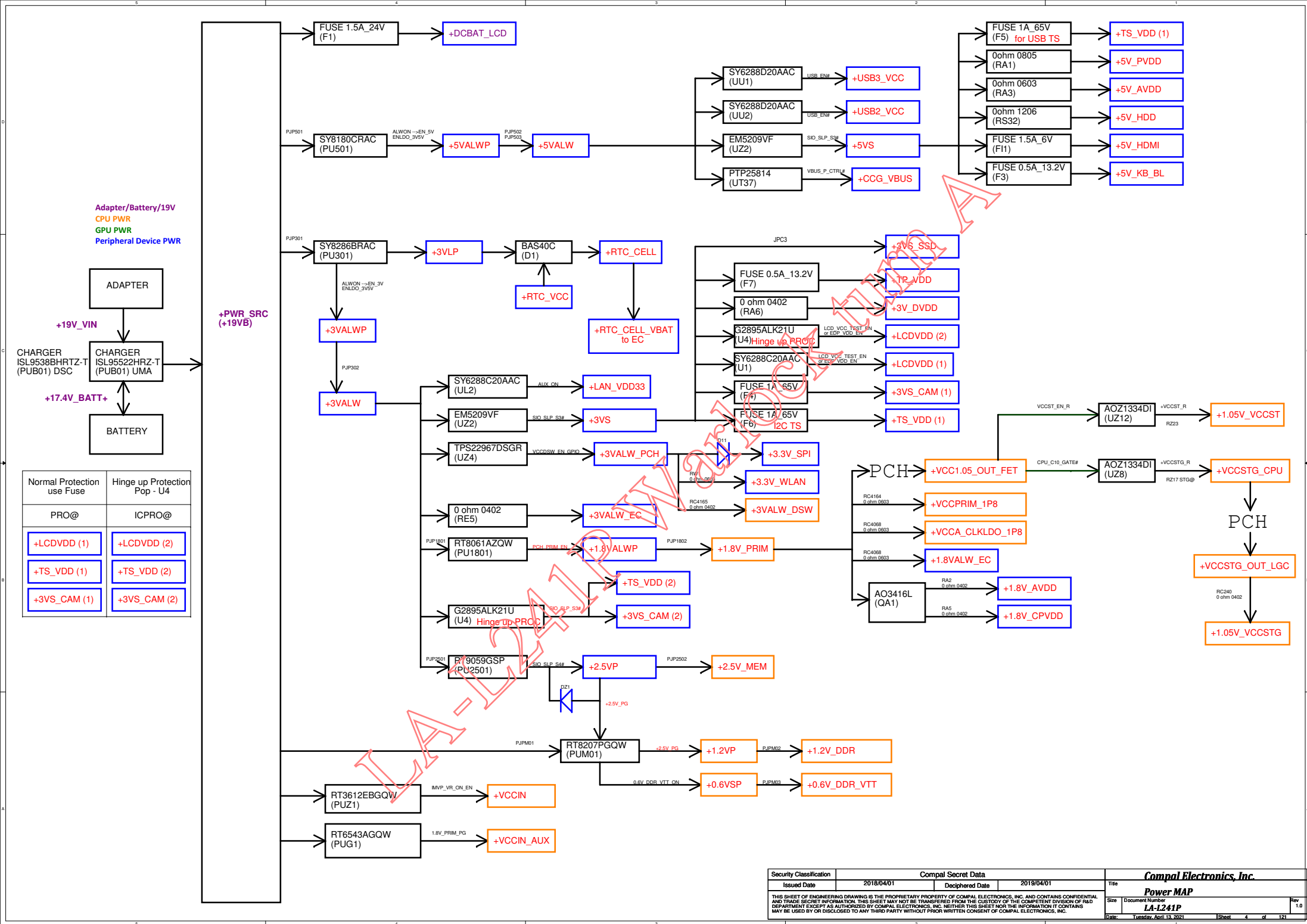
Figure 77. High Speed I/O (HSIO) Lane Multiplexing in PCH-LP (UP3)

Flex HSIO Lane	0	1	2	3	4	5	6	7	8	9	10	11
HSIO Type and Lane	USB 3.2 Gen 1x1/2x1 #1	USB 3.2 Gen 1x1/2x1 #2	USB 3.2 Gen 1x1/2x1 #3	USB 3.2 Gen 1x1/2x1 #4	PCIE* #5	PCIE* #6	PCIE* #7	PCIE* #8	PCIE* #9	PCIE* #10	PCIE* #11	PCIE* #12

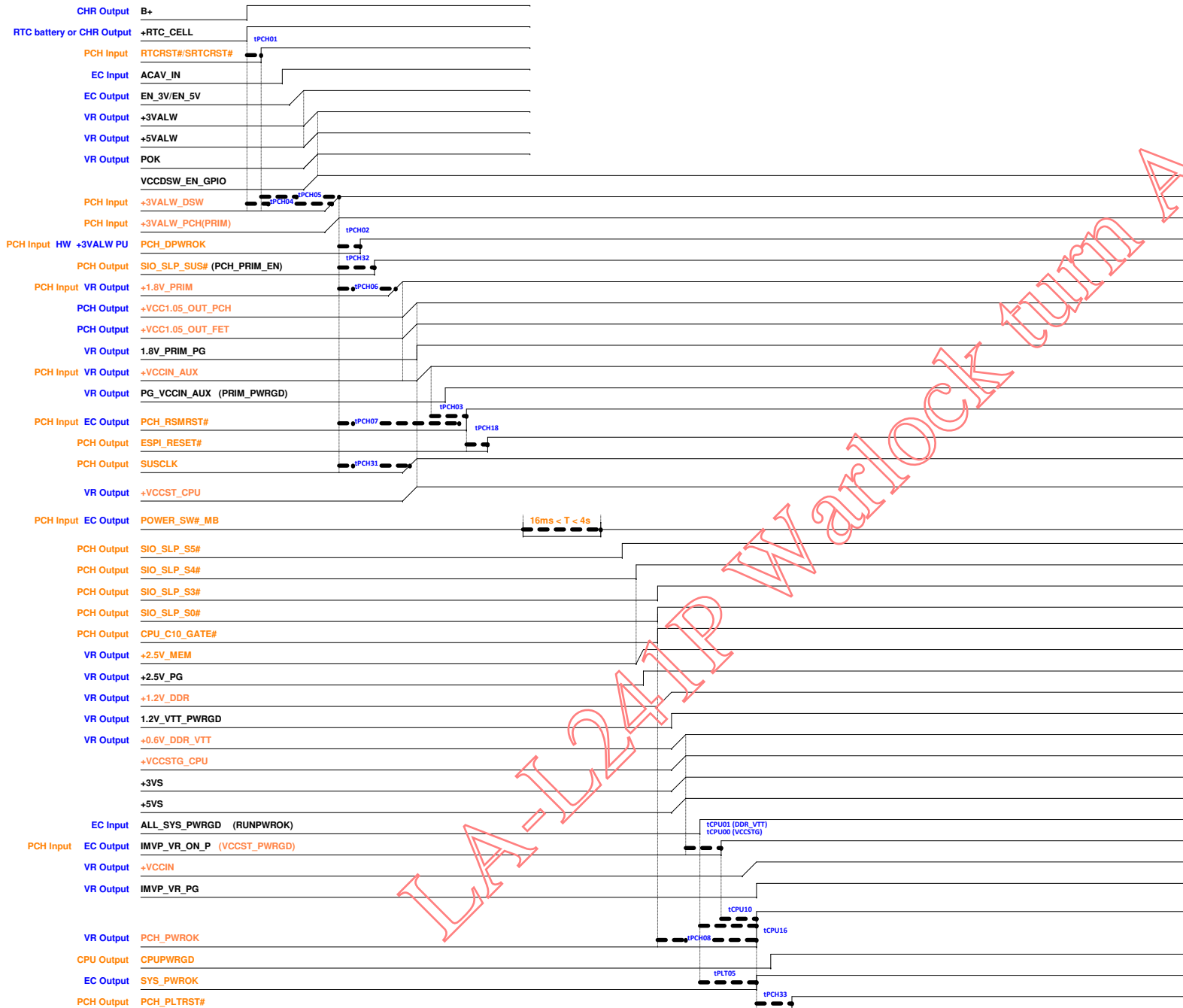
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				Version: 1.0

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Power Up Sequence  
G3 to S0



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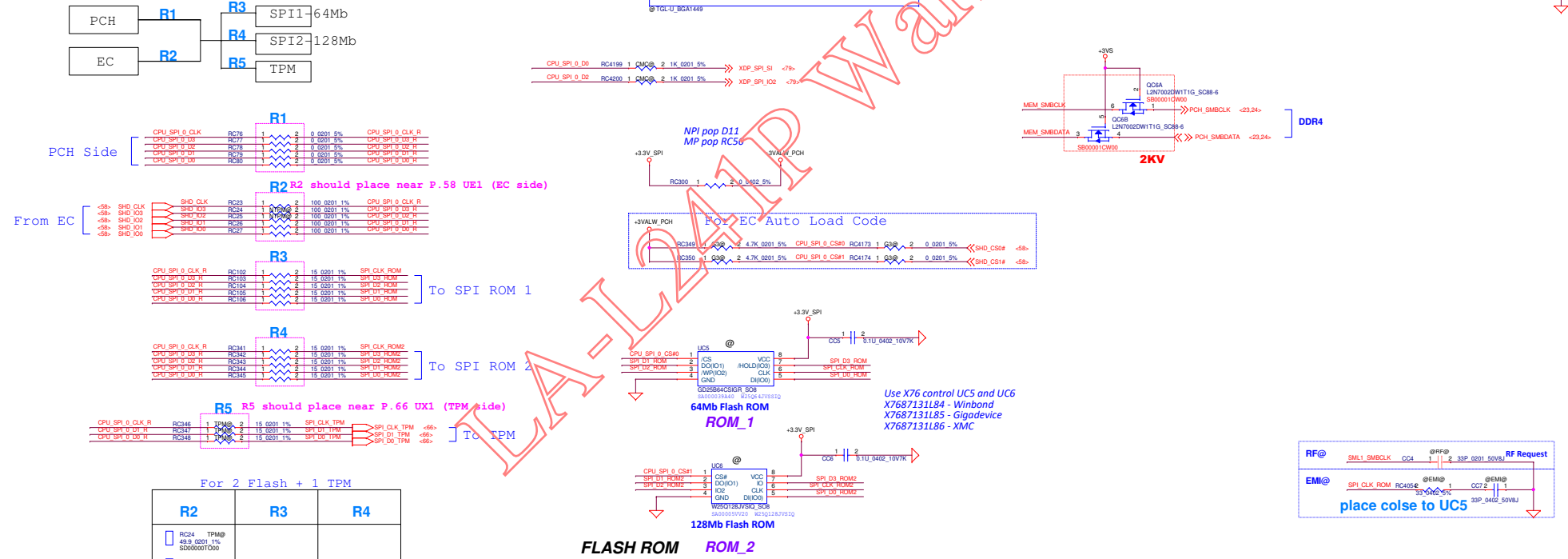
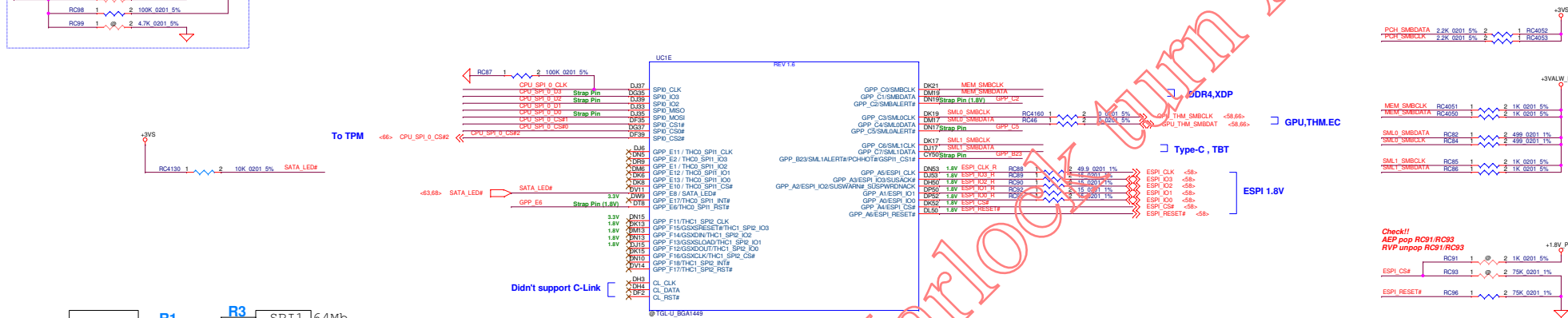
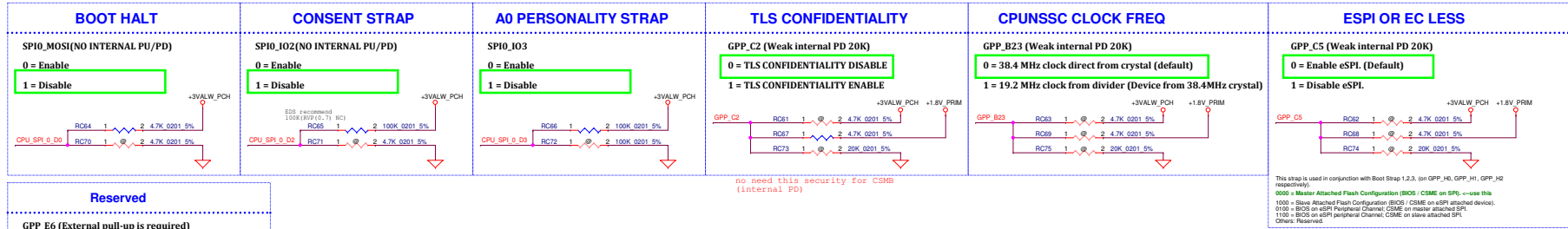










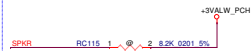


## TOP SWAP OVERRIDE

GPP\_B14 / SPKR (Internal 20 K Pull Down)

0 = Disable "Top Swap" mode. (Default)

1 = Enable "Top Swap" mode.

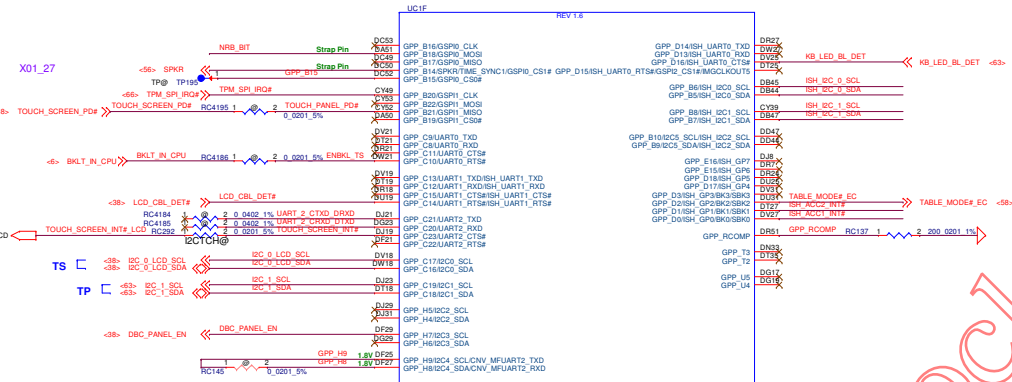


## NO REBOOT

GPP\_B18/GSPI0\_MOS (Internal 20 K Pull Down)

0 = REBOOT ENABLED

1 = NO REBOOT (This function is useful when running ITP/XDP).



Reserved for Gi/Gyo  
Reserve for FFS

ISH GPP for Main Accelerometer (I2C Board/NTA)  
ISH GPP for 2nd Accelerometer (I2C Board/NTA)  
ISH GPP for Table MODE#  
ISH GPP for ALS, Ambient  
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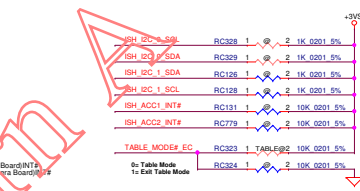
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Flash Descriptor Security Override

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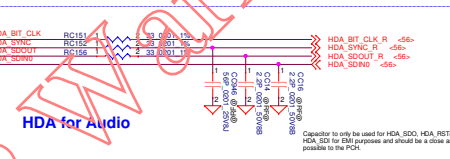
Flash Descriptor Security Override

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Flash Descriptor Security Override



HDA for Audio

HDA for Audio

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HDA for Audio

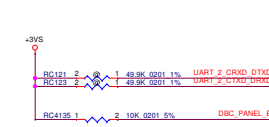
HDA for Audio

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Place near JWLAN1



BT RADIO DIS

BT RADIO DIS

BT RADIO DIS

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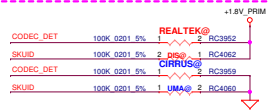
BT RADIO DIS

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REALTEK CODEC\_DET

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REALTEK CODEC\_DET

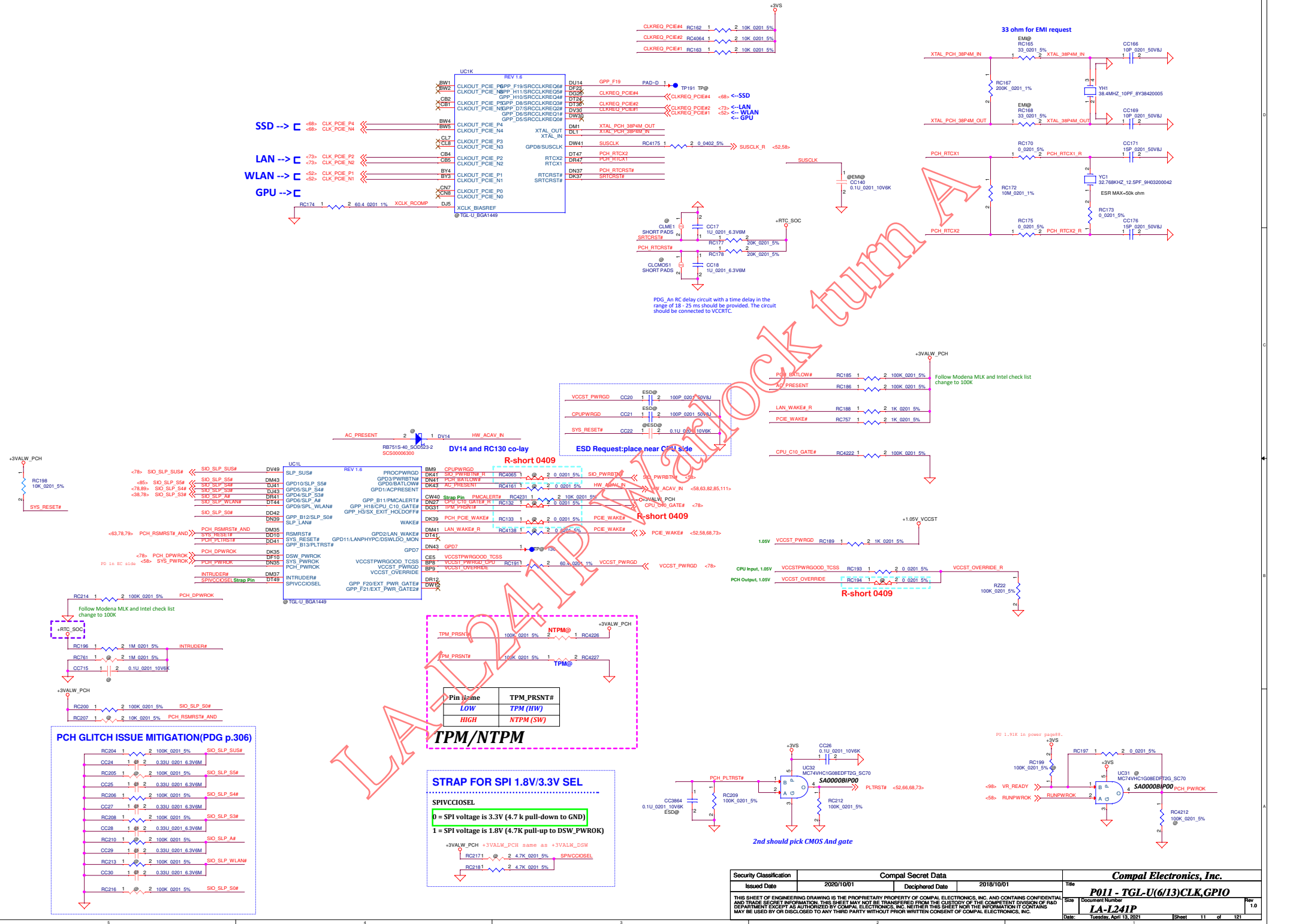
Pin Name	CODEC_DET
Main Realtek Codec	HIGH REALTEK@
2nd Cirrus Codec	LOW CIRRUS@

N3/V3

SKUID	UMA@	LOW
	DIS@	DSC

From eDP	
Pin Name	DPST_EN
HIGH	120 Hz Panel
LOW	60 Hz Panel

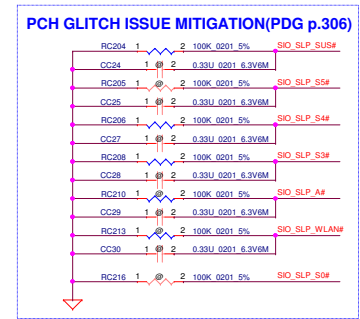
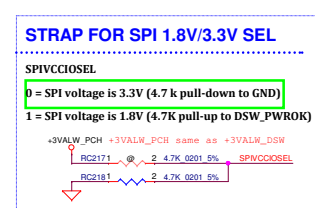
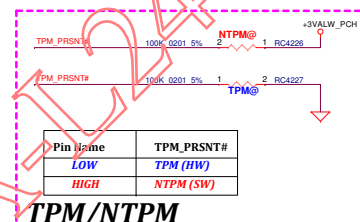
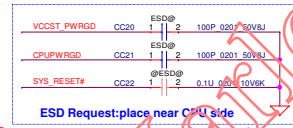
From DB to PCH	
Pin Name	N3V3_DET
HIGH	N3 non-LAN
LOW	V3 LAN



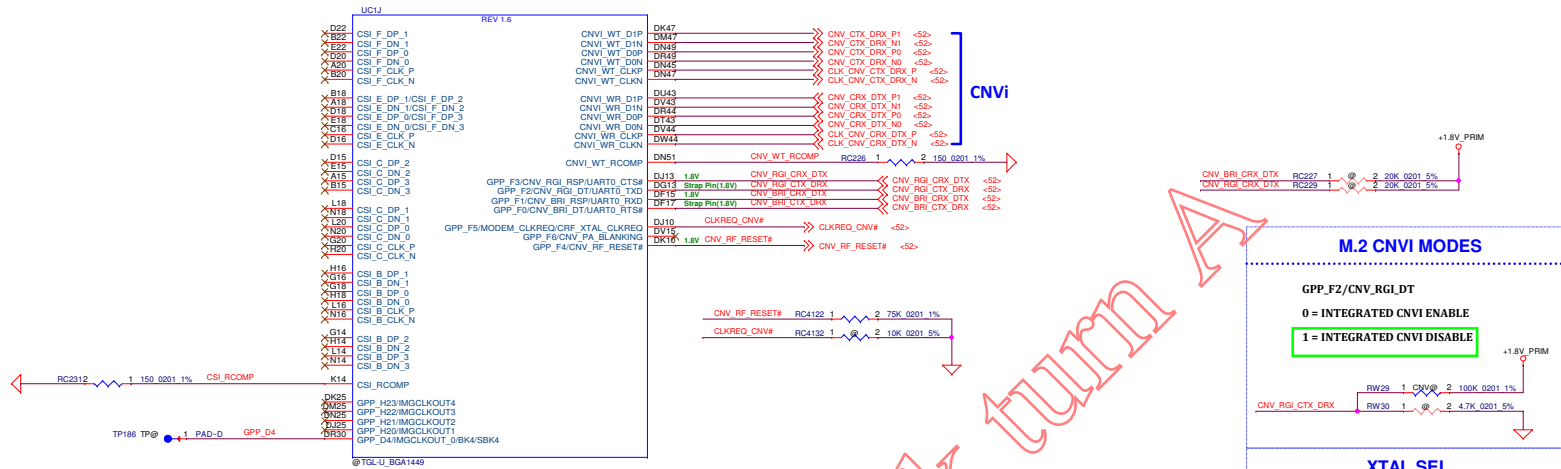
SSD --> C  
LAN --> C  
WLAN --> C  
GPU --> C

33 ohm for EMI request

PDG\_An RC delay circuit with a time delay in the range of 18-25 ns should be provided. The circuit should be connected to VCCRTC.

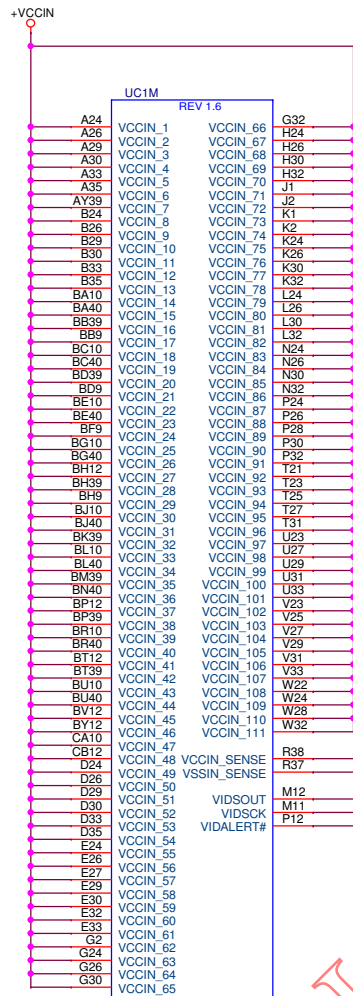




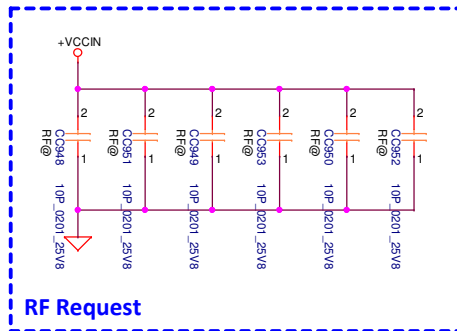


LA-L241P Warlock turn A

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@TGL-U\_BGA1449



RF Request

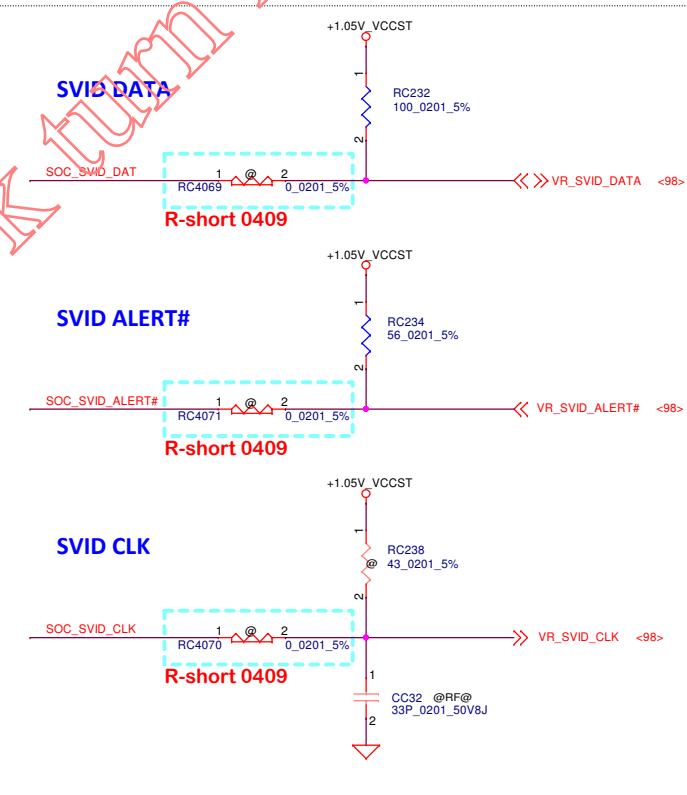
Trace Length Match < 25 mils  
Must be routed as differential pair to VR

VCC\_SENSE\_VCCIN <98>  
VSS\_SENSE\_VCCIN <98>

SOC\_SVID\_DAT  
SOC\_SVID\_CLK  
SOC\_SVID\_ALERT#

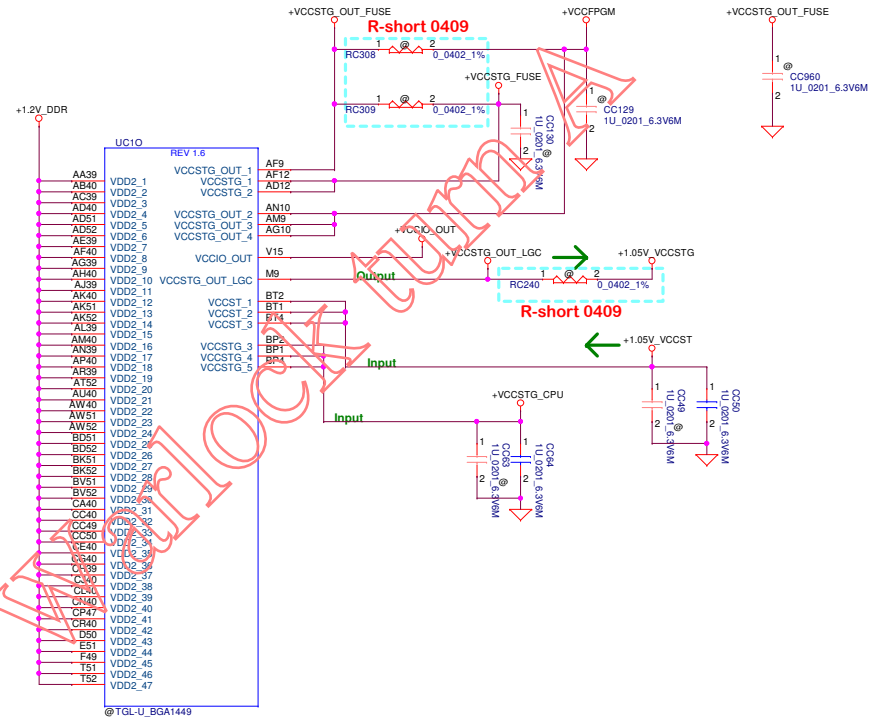
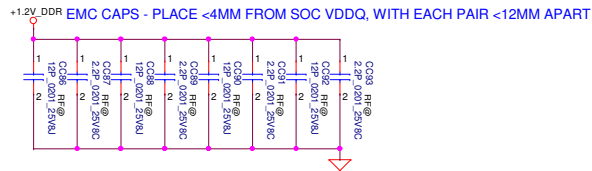
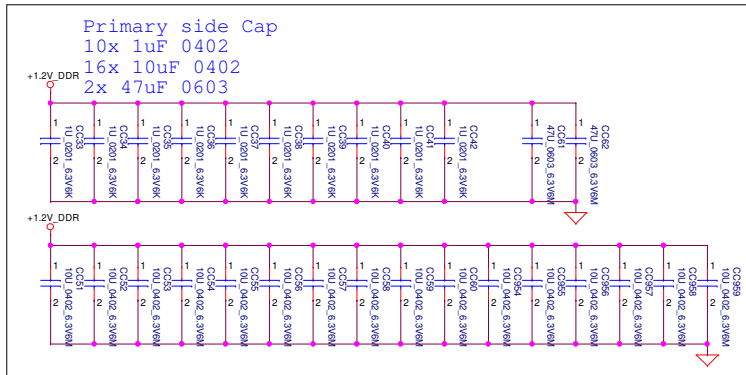
1. The total Length of Data and Clock (from CPU to each VR) must be equal ( $\pm 0.1$  inch).
2. Route the Alert signal between the Clock and the Data signals.

CAD Note: Place the PU resistors close to CPU



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Issued Date	2020/10/01	Deciphered Date	2018/10/01	P014 - TGL-U(9/13)CPU PWR,SVID	
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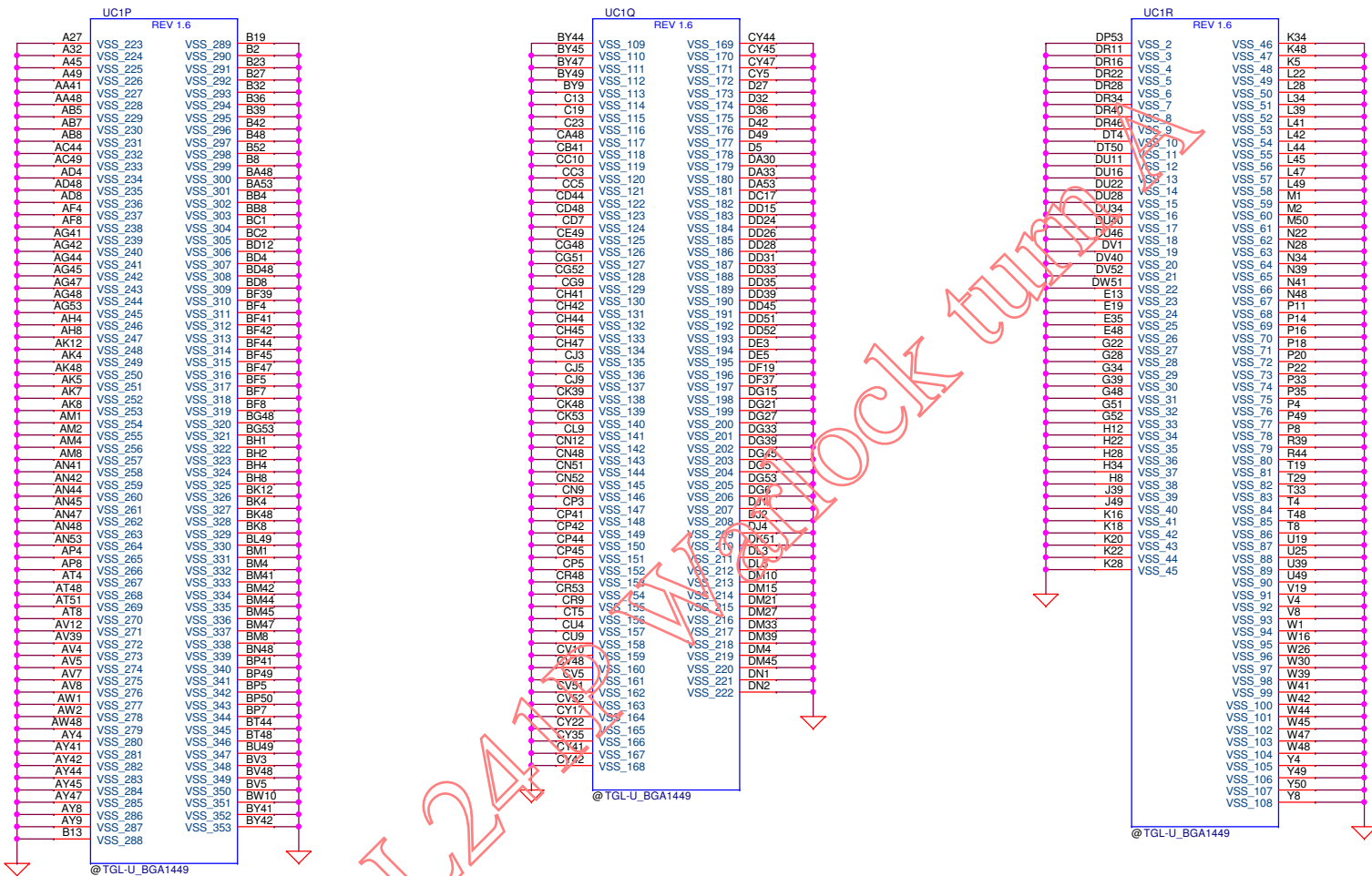




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				Rev	1.0
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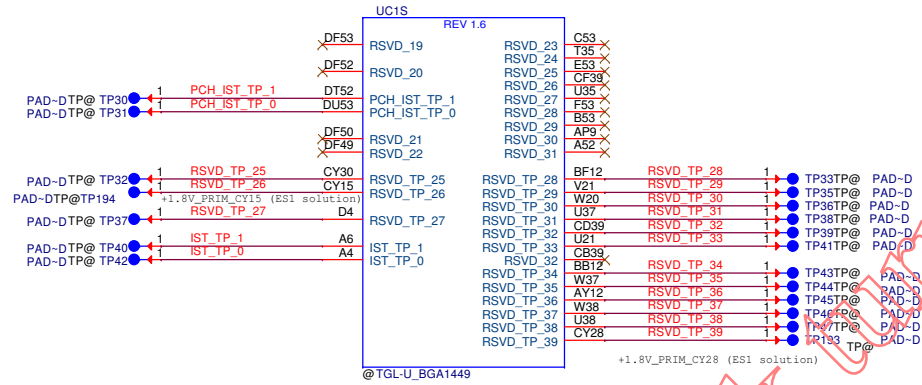






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						Size		Document Number		Rev	
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ES1 Workaround Circuit  
Intel Document Number: 614056



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Size		Document Number			Rev
Date		Tuesday, April 13, 2021			1.0
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Main Function:

Reserve

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				LA-K033P	1.0
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					LA-L241P	1.0
				Date:	Tuesday, April 13, 2021	Sheet 21 of 121

Main Function:

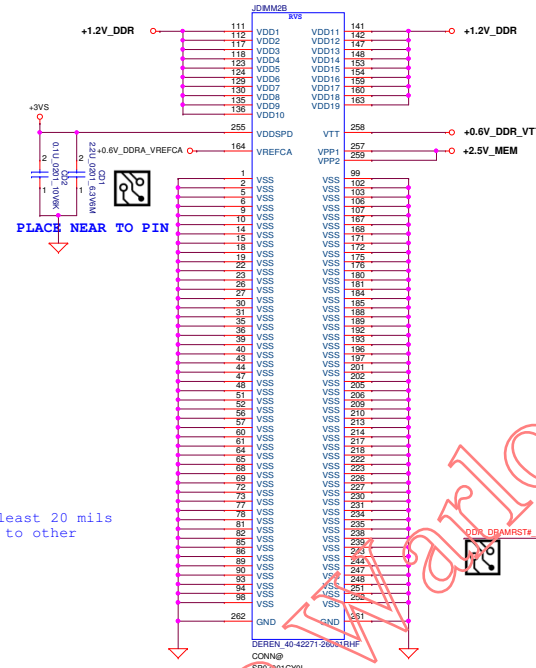
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					LA-K032P	1.0
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## Non-Interleaved Memory

[illegible]

The diagram illustrates the VREF traces for the DIMM and CPU sides. On the DIMM Side, a 1.2V\_DDR supply is connected to a network of resistors (RD9, RD10, RD11) and a capacitor (C10). The CPU Side features a +V\_DDR\_REFA\_R supply connected to a network of resistors (RD10, RD12) and a capacitor (CDS). The traces are labeled with their respective component values and are shown with a 20 mil spacing.

**DIMM Side**

+0.6V\_DDRA\_VREFCA

1.2V\_DDR

RD9 1K\_0402\_1%

RD10 2.0402\_1%

RD11 1K\_0402\_1%

**CPU Side**

+V\_DDR\_REFA\_R

RD10 2.0402\_1%

RD12 24.9\_0402\_1%

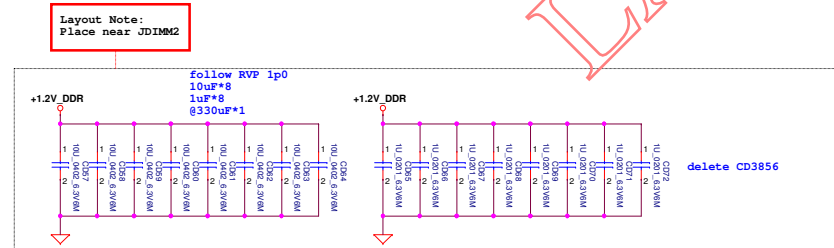
CDS 0.022U\_0201\_25V8K

VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

**Diagram 1: +2.5V\_MEM**  
 Layout Note: Place near JDIMM2.257,259  
 Schematic: A 10uF capacitor (C0402) and a 1uF capacitor (C0402) are connected in parallel between the +2.5V\_MEM plane and ground. The capacitors are placed near the JDIMM2.257 and JDIMM2.259 pins. The ground connection is marked with a red triangle and a red 'A'.

**Diagram 2: +0.6V\_DDR\_VTT**  
 Layout Note: Place near JDIMM2.258  
 Schematic: A 10uF capacitor (C0402) and a 1uF capacitor (C0402) are connected in parallel between the +0.6V\_DDR\_VTT plane and ground. The capacitors are placed near the JDIMM2.258 pin. The ground connection is marked with a red triangle and a red 'A'.

**Diagram 3: +0.6V\_DDR\_VREFCA**  
 Layout Note: PLACE THE CAP near JDIMM2. 164  
 Schematic: A 2.2uF capacitor (C0402) and a 0.1uF capacitor (C0402) are connected in parallel between the +0.6V\_DDR\_VREFCA plane and ground. The capacitors are placed near the JDIMM2.164 pin. The ground connection is marked with a red triangle and a red 'A'.



POP  
EMI@  
UNPOP  
@EMI@\\@ESD@\\@RF@\\CONN@\\@

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				Date:	Tuesday, April 13, 2021	Sheet 25 of 121

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					LA-L241P	1.0
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Main Func = GPU

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Issued Date	2018/08/31	Deciphered Date	2019/08/06	NV(1/5)-PCIE	
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Main Func = GPU

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Main Func = GPU

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Main Func = GPU



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Main Func = GPU

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Main Func = VRAM

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Main Func = VRAM

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				Tuesday, April 13, 2021	1.0
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Main Func = CAM&MIC, TS



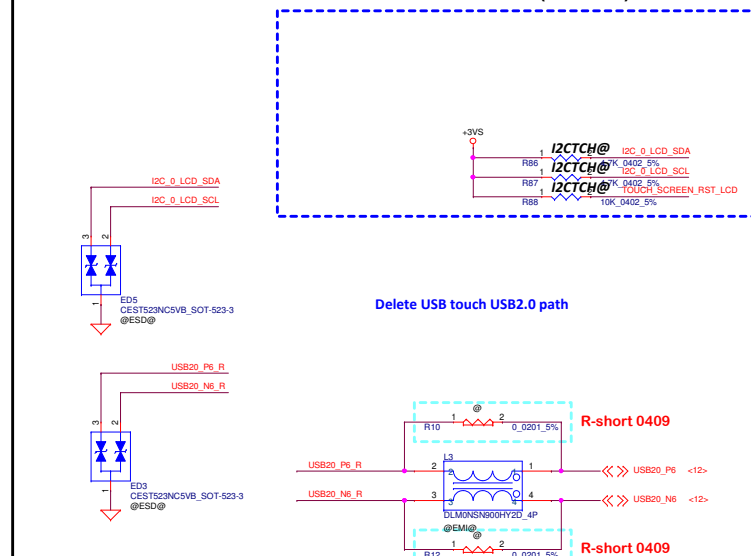
Delete +MIC\_VCC PWR rail

### Delete 3V Cam Fuse

**Non-TCH -->R81, R82, F5 unpop**

[illegible]

## I2C Touch Screen (Reserved)



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Date: Tuesday, April 13, 2019				Sheet	38 of 121	

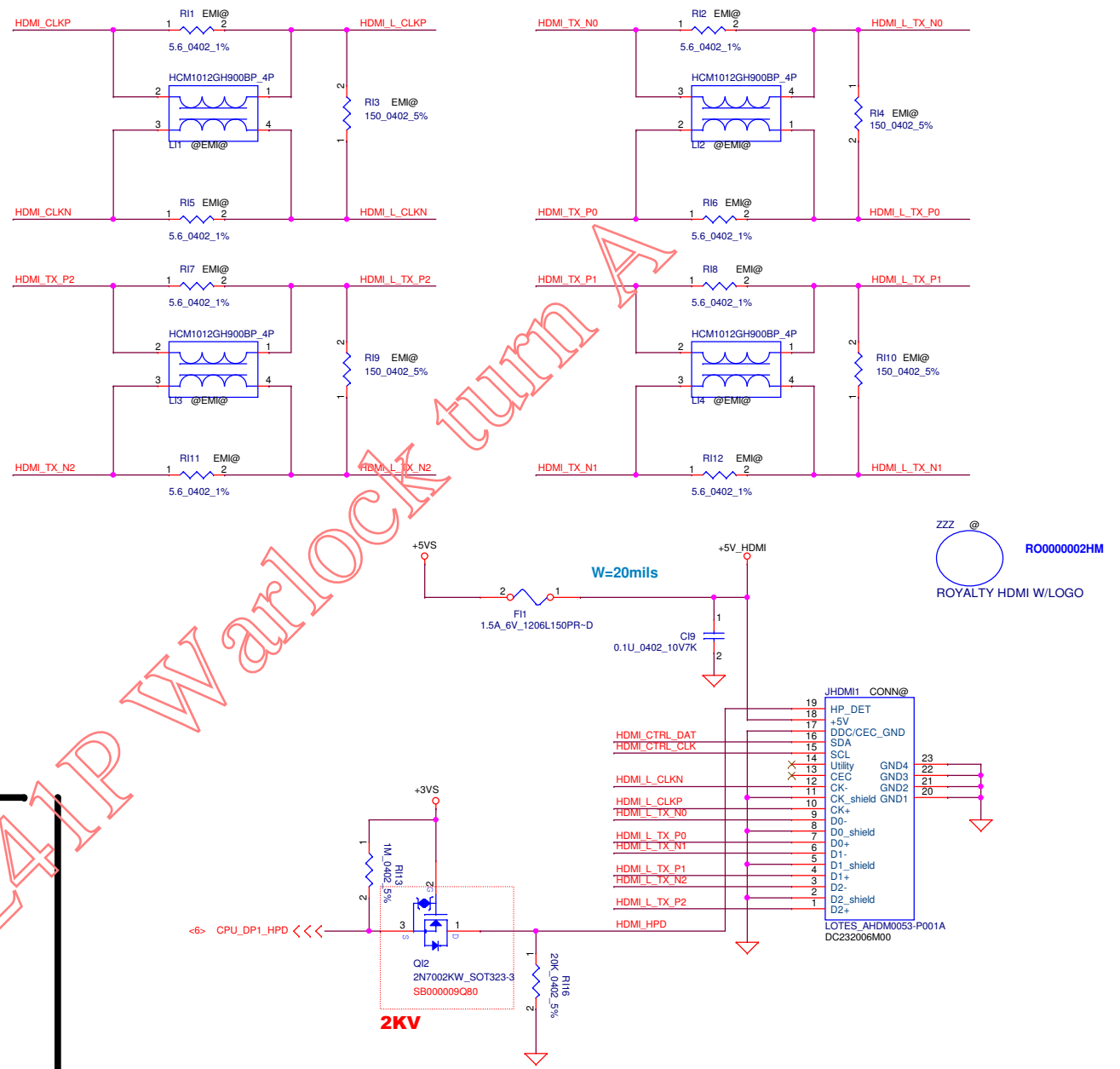
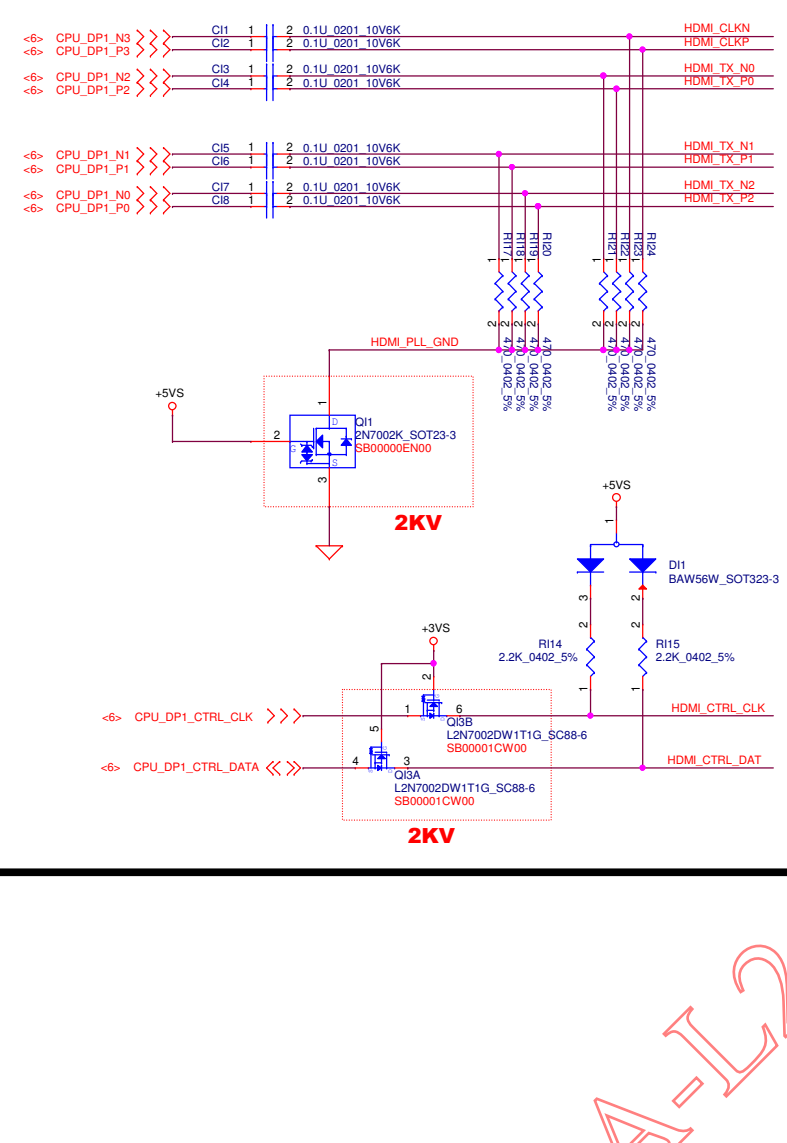
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Main Func = HDMI



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		LA-1241P			
		Date: Tuesday, April 19, 2021			
		[Sheet 42 of 121]			
		Rev 1.0			

Compal Electronics, Inc.

TBT TYPE-C Port0 (1/2)

LA-L241P

Tuesday, April 13, 2021

42

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Main Func =

Reserve

LA-L241P Warlock turn A

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Issued Date	2018/12/24	Deciphered Date	2018/12/31	Title	TBT TYPE-C Port0 (2/2)
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				Date	Tuesday, April 13, 2021
				Sheet	43 of 121

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				Size	
				Document Number	
				Rev	
				1.0	
		Date		Tuesday, April 19, 2021	
		[Sheet]		44 of 121	



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				Date	Tuesday, April 13, 2021
				Sheet	45 of 121
				Rev	1.0
				LA-L241P	

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				Rev	1.0
				LA-L241P	

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		Date		Tuesday, April 13, 2021	
		Sheet		47 of 121	

Reserve

LA-L241P Wallock turn A

LA-L241P Warlock turn A

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				Rev	1.0

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				LA-1241P			
				Date:	tuesday, april 13, 2021	Sheet	50 of 121

Main Func = LAN

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				Date: Tuesday, April 13, 2021	Sheet 51 of 121

## Main Func = WLAN

## E Key CONN



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Reserve

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				Date:	Tuesday, April 13, 2021	Sheet 53 of 121

Main Function:

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					LA-L241P	1.0
				Date:	Tuesday, April 13, 2021	Sheet 54 of 121

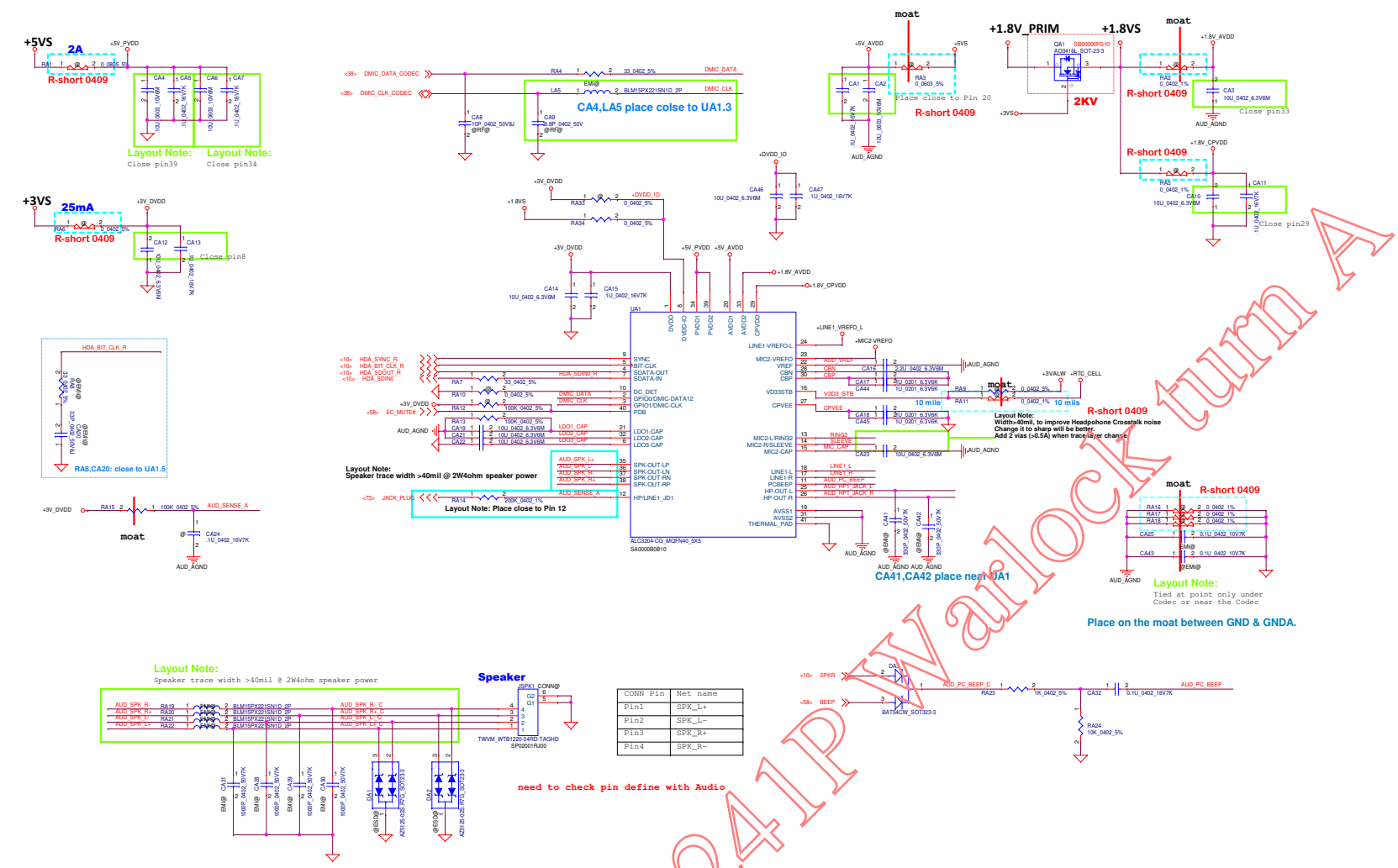
Main Function:

Reserve

LA-L241P Warlock turn A

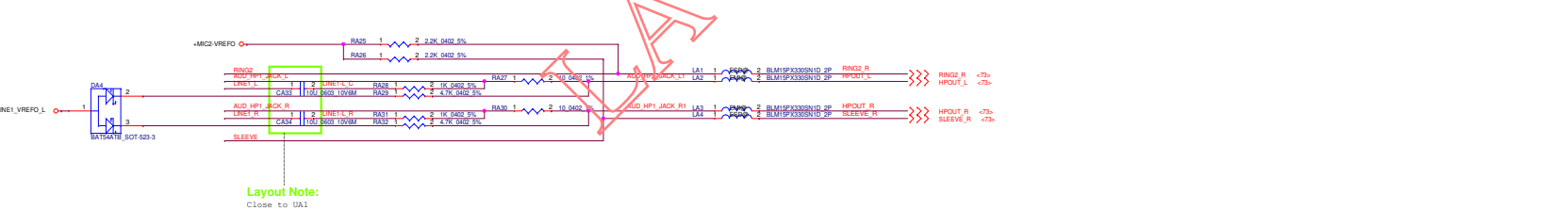
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title	(RSVD)	
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Main Func = Audio



Main Func = Audio Jack

Universal Jack  
(Global Headset Jack + mic phone in + line in support)



Main Function:

Reserve




LA-L241P Warlock turn A

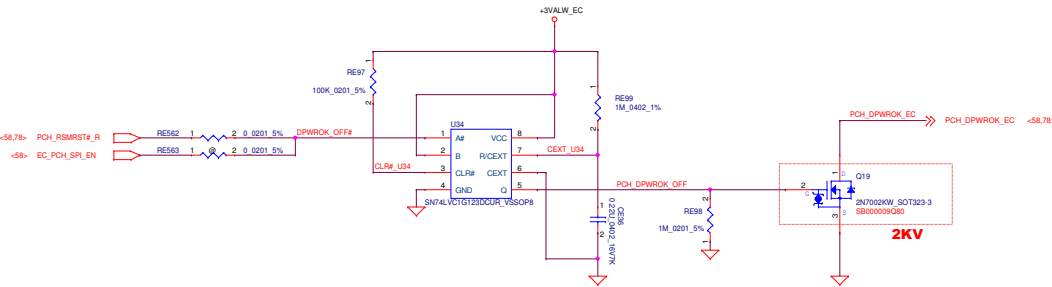
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Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title	(RSVD)	
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					LA-L241P	1.0
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			LA-L241P	Rev 1.0

Main Function: WDT circuit

FUNCTION TABLE

INPUTS			OUTPUTS
CLR	A	B	Q
L	X	X	L
X	H	X	L <sup>(1)</sup>
X	X	L	L <sup>(1)</sup>
H	L	↑	
H	↓	H	
↑	L	H	



t <sub>OUT</sub> <sup>(2)</sup>	Q	C <sub>int</sub> = 28 pF, R <sub>int</sub> = 2 kΩ	225	600	190	220	170	200	150	180	ns
		C <sub>int</sub> = 0.01 μF, R <sub>int</sub> = 10 kΩ	100	110	100	110	100	110	100	110	μs
		C <sub>int</sub> = 0.1 μF, R <sub>int</sub> = 10 kΩ	1	1.1	1	1.1	1	1.1	1	1.1	ms

Main Function: S5 LID

Main Function:

Reserve

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0

JeDP CONN  
For Touch Screen



NGT7718W I<sup>2</sup>C/ SMBus™ address is 1001100xb (x is R/W bit)

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SMBus Address: 1001100xb (x is R/W bit)


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## Appendix C. SMBus Device Address Assignments

0101 500	X	Reserved for continuous extension of the
----------	---	--

0101 500 X Reserved by

\_\_\_\_\_

2	1
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Main Function:

Reserve

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Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title	(RSVD)	
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Main Function:

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					LA-L241P	1.0
				Date:	Tuesday, April 13, 2021	Sheet 64 of 121

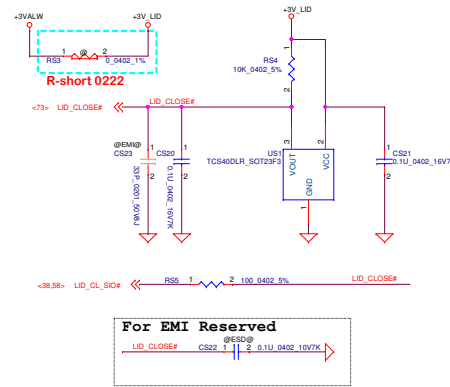
Main Function:

Reserve

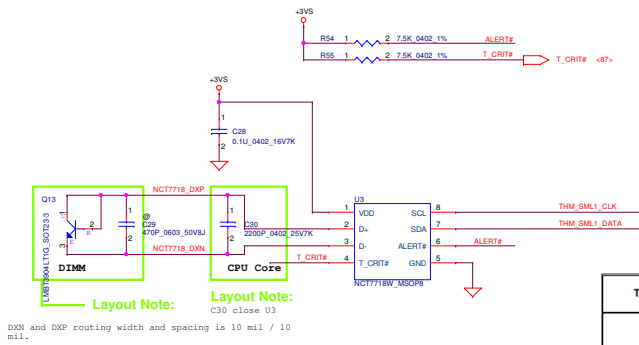
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# Main Func = Hall Sensor

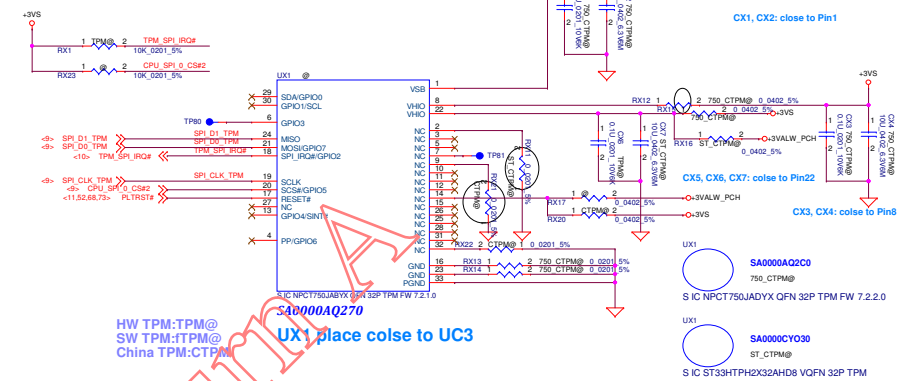


# Main Func = Thermal

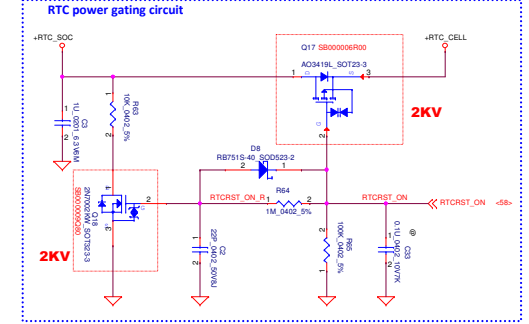


TEMPERATURE (°C)	T_CRIT#				
	2KQ	7.5KQ	10.5KQ	14KQ	18.7KQ
ALERT#	2KQ	77	87	97	107
	7.5KQ	79	89	99	109
	10.5KQ	81	91	101	111
	14KQ	83	93	103	113
	18.7KQ	85	95	105	115

# Main Func = TPM

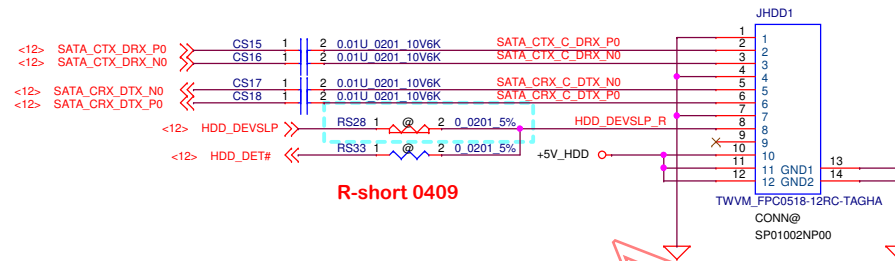
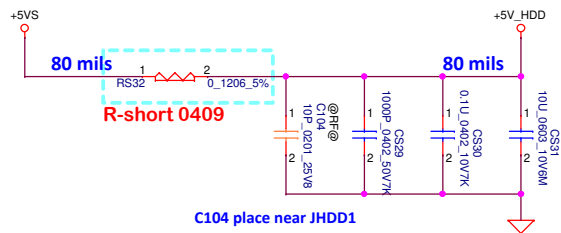


# Main Func = RTC



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Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title	TPM/RTC/Screw hole
Size	Document Number	LA-K032P	Rev	1.0	
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Main Func = HDD&FFS



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	8
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	9

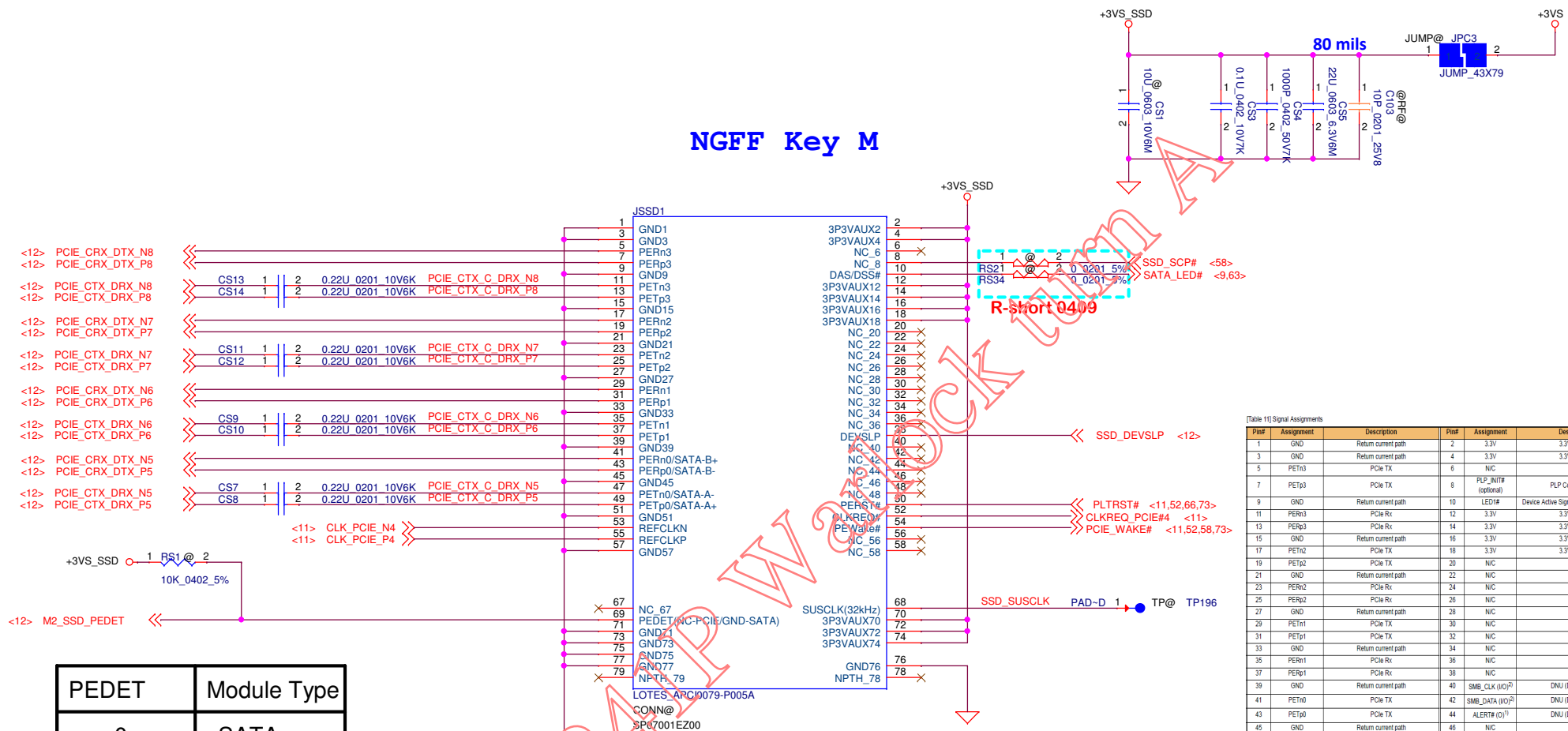
Main Func = ODD

Cancel ODD

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				Tuesday, April 13, 2021		1.0	
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M Key CONN

## NGFF Key M



PEDET	Module Type
0	SATA
1	PCIE

Pin#	Assignment	Description	Pin#	Assignment	Description
1	GND	Return current path	2	3.3V	3.3V source
3	GND	Return current path	4	3.3V	3.3V source
5	PETn3	PcIe TX	6	NIC	NIC
7	FETp3	PcIe TX	8	PLP_INIT# (OPTION)	PLP Control Signal
9	GND	Return current path	10	LED1#	Device Active Signal (Refer to [Table 12])
11	PERn3	PcIe Rx	12	3.3V	3.3V source
13	PERp3	PcIe Rx	14	3.3V	3.3V source
15	GND	Return current path	16	3.3V	3.3V source
17	PETn2	PcIe TX	18	3.3V	3.3V source
19	PETp2	PcIe TX	20	NIC	NIC
21	GND	Return current path	22	NIC	NIC
23	PERn2	PcIe Rx	24	NIC	NIC
25	PERp2	PcIe Rx	26	NIC	NIC
27	GND	Return current path	28	NIC	NIC
29	PETn1	PcIe TX	30	NIC	NIC
31	PETp1	PcIe TX	32	NIC	NIC
33	GND	Return current path	34	NIC	NIC
35	PERn1	PcIe Rx	36	NIC	NIC
37	PERp1	PcIe Rx	38	NIC	NIC
39	GND	Return current path	40	SMB_CLK (I/O) <sup>2</sup>	DNU (Do Not Use)
41	PETn0	PcIe TX	42	SMB_DATA (I/O) <sup>2</sup>	DNU (Do Not Use)
43	PETp0	PcIe TX	44	ALERT# (I/O) <sup>1</sup>	DNU (Do Not Use)
45	GND	Return current path	46	NIC	NIC
47	PERn0	PcIe Rx	48	NIC	NIC
49	PERp0	PcIe Rx	50	PERS1#	PcIe Reset
51	GND	Return current path	52	CLKREQ#	PcIe Device Clock Request
53	REFCLKN	PcIe Reference Clock	54	PEWAKE#	NIC
55	REFCLKP	PcIe Reference Clock	56	Reserved for MFG_2 Data	DNU (Do Not Use)
57	GND	Return current path	58	Reserved for MFG_2 CLOCK	DNU (Do Not Use)
67	NIC	NIC	68	SUSCLK	DNU (Do Not Use)
69	PEDET	NIC	70	3.3V	3.3V source
71	GND	Return current path	72	3.3V	3.3V source
73	GND	Return current path	74	3.3V	3.3V source
75	GND	Return current path			

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Main Func = eMMC

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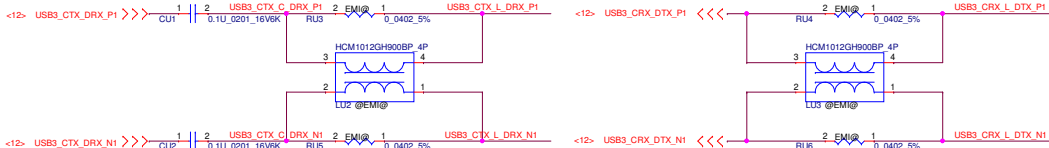
Main Function:

Reserve

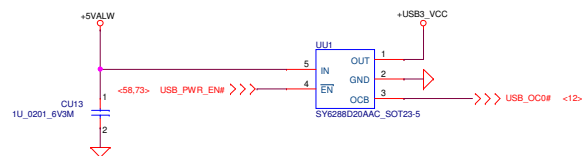
LA-L241P Wallock turn A

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					LA-L241P	1.0
				Date:	Tuesday, April 13, 2021	Sheet 70 of 121

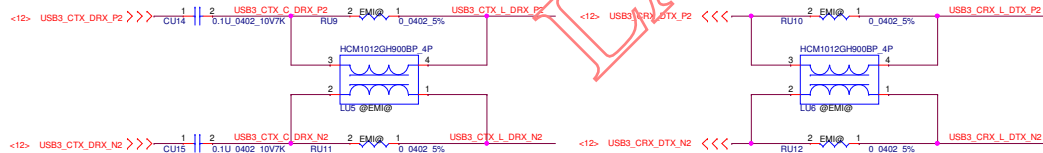
**Main Func = USB3.0 Port1**



Maximum Output Current 2A



**Main Func = USB3.0 Port2**



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Main Function:

Reserve

LA-L241P Warlock turn A

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Main Function:

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Main Function:

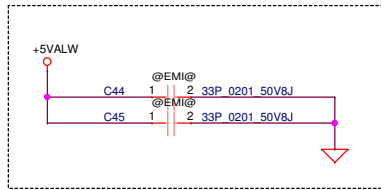
Reserve

LA-L241P Warlock turn A

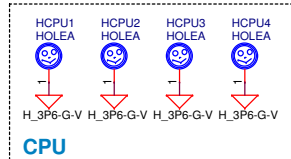
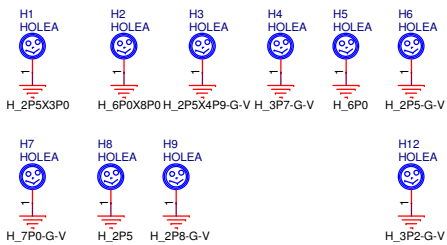
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				Date:	Tuesday, April 13, 2021	Sheet 76 of 121



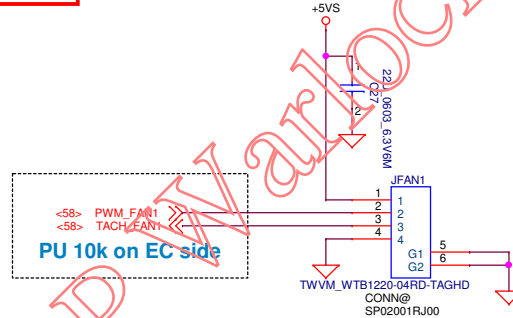
# EMI reserve bridge



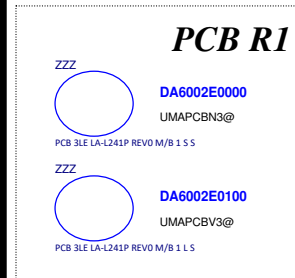
## Screw hole/FD



## FAN



## PCB PN



## PCB DAZ R1



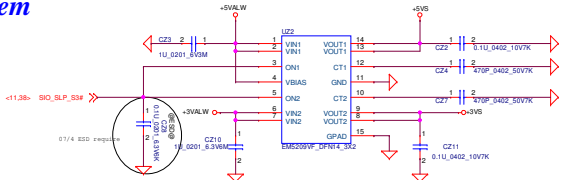
## PCB DAZ R3



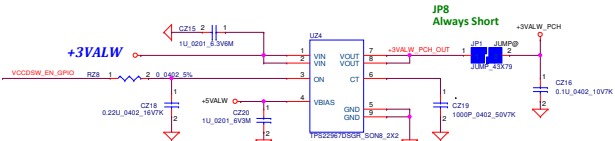
1029 ME update

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				Date:	Wednesday, April 14, 2021	Sheet 77 of 121

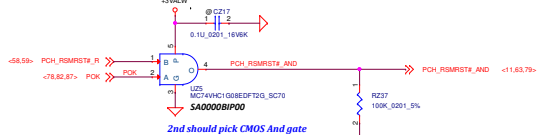
+5VS / +3VS for System



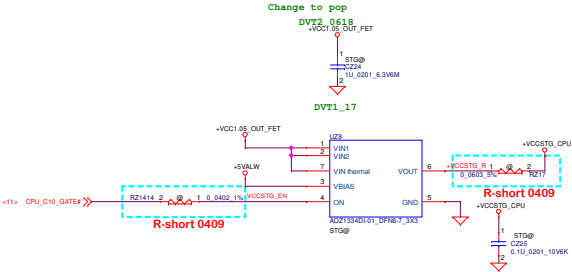
+3VALW TO +3VALW\_PCH



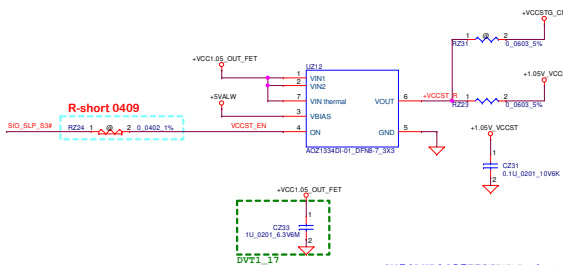
RSMRST circuit



VCCSTG



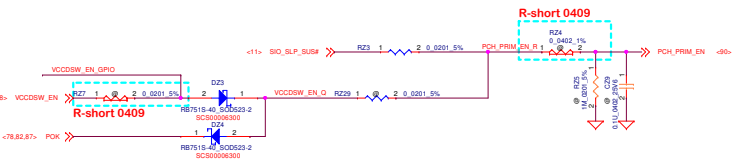
+1.2V\_VDDQ TO +1.2V\_VCCPLL\_OC



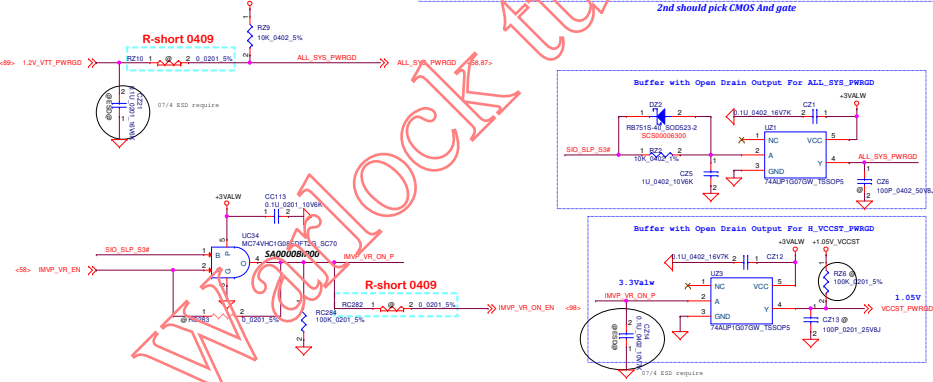
SN74AUP1C FUNCTION TABLE

INPUTS		OUTPUT
C	B	A
L	L	L
L	L	H
L	H	L
L	H	H
H	L	L
H	L	H
H	H	L
H	H	H

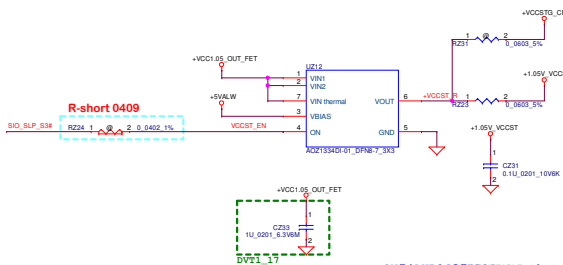
Sequence Logic



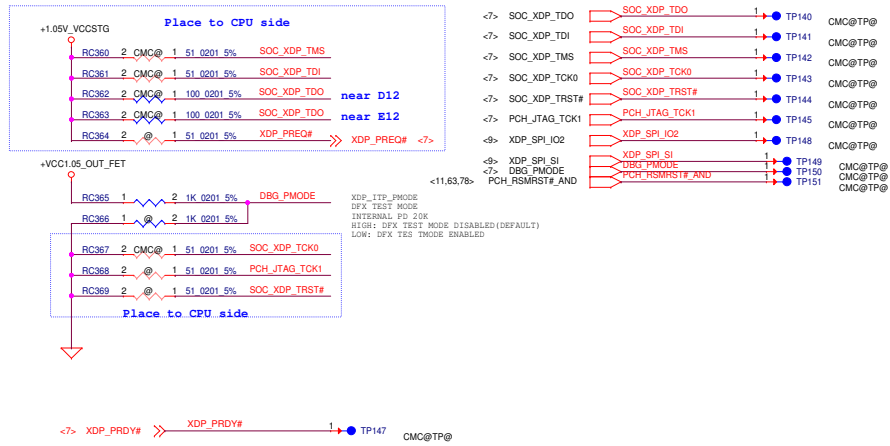
IMVP\_VR\_ON&VCCST\_PWRGD



VCCST



Main Func = Debug connector



LA-L241P Warlock turn A

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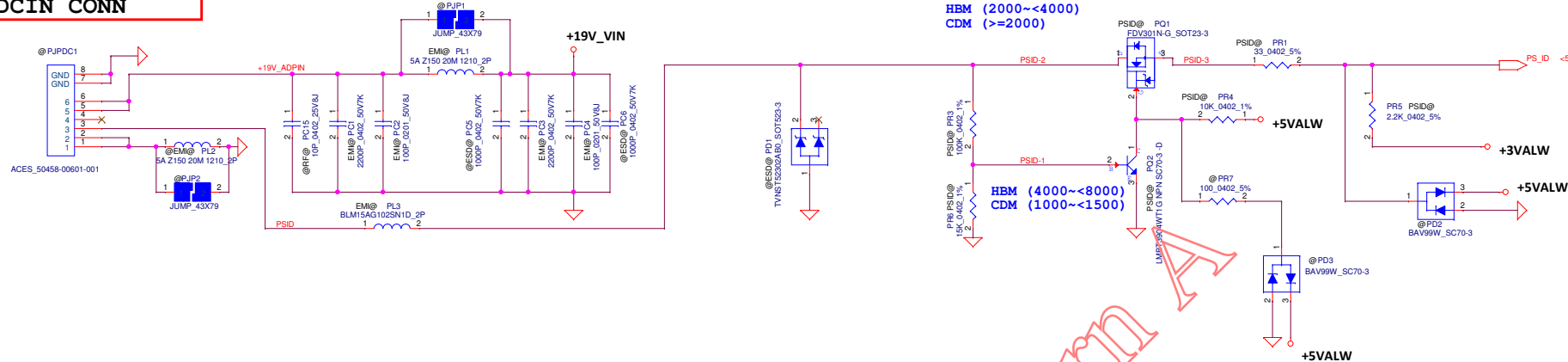
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				Size	Document Number	0.1
Date: Tuesday, April 13, 2021				Sheet	81	of 121

# Main Func = DCIN CONN



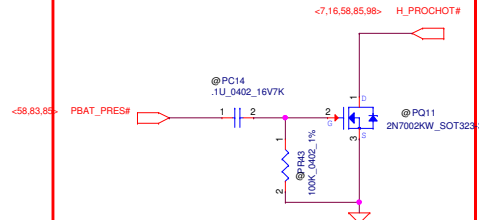
## Battery Bot Side

PIN1 GND  
PIN2 GND  
PIN3 GND  
PIN4 SYS\_PRES  
PIN5 BATT\_PRS  
PIN6 DAT\_SMB  
PIN7 CLK\_SMB  
PIN8 Batt+  
PIN9 Batt+  
PIN10 Batt+  
SP021412220

ACES\_50458-01001-P01\_10P-T

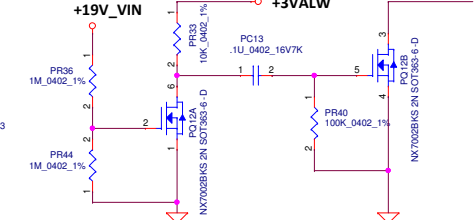
### Adapter protection:

if battery removed, adaptor only,  
then trigger the H\_PROCHOT#,  
keep it in BOM since battery can not  
be removed by end user

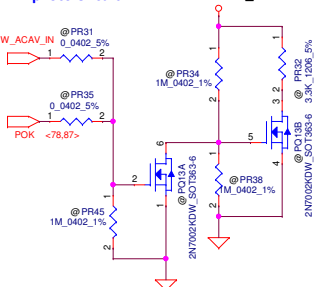


### Battery protection:

asserts H\_PROCHOT# when adaptor is  
unplugged, keep low for 10ms  
till SW PROCHOT# is issued by EC



### Erp lot6 Circuit



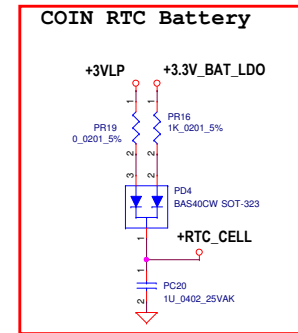
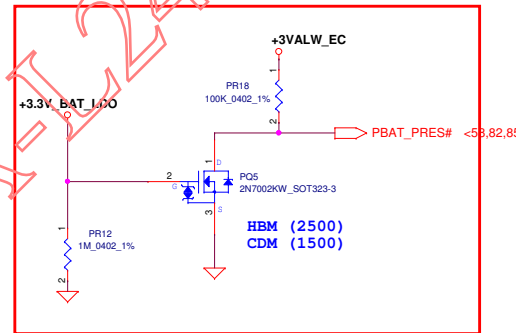
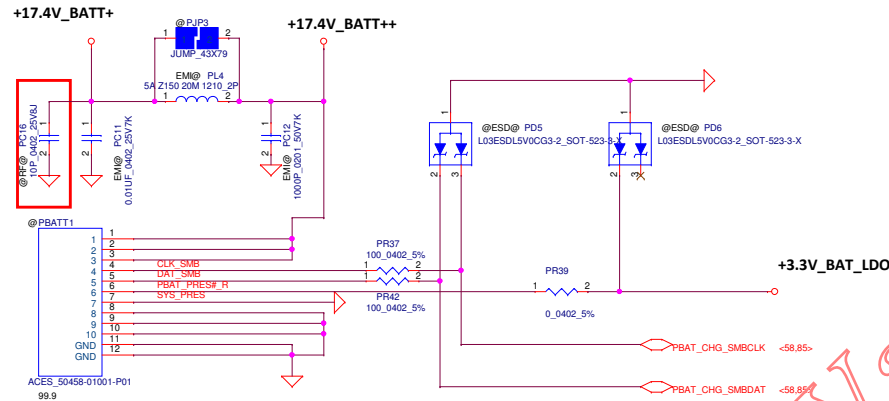
Security Classification				Compal Secret Data				DELL CONFIDENTIAL/PROPRIETARY			
Issued Date				Deciphered Date				Compal Electronics, Inc.			
2018/04/01				2019/04/01				PWR_DCIN CONN			
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Main Func = BATT CONN

Battery Bot Side

PIN1 GND  
PIN2 GND  
PIN3 GND  
PIN4 SYS\_PRES  
PIN5 BATT\_PRS  
PIN6 DAT\_SMB  
PIN7 CLK\_SMB  
PIN8 Batt+  
PIN9 Batt+  
PIN10 Batt+  
SP021412220

ACES\_50458-01001-P01\_10P-T



Security Classification		Compal Secret Data		DELL CONFIDENTIAL/PROPRIETARY	
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2018/04/01		2019/04/01		Title	
				PWR_BATT CONN	
				Document Number	
				Rev	
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				Date: Tuesday, April 13, 2021	
				Sheet 83 of 121	

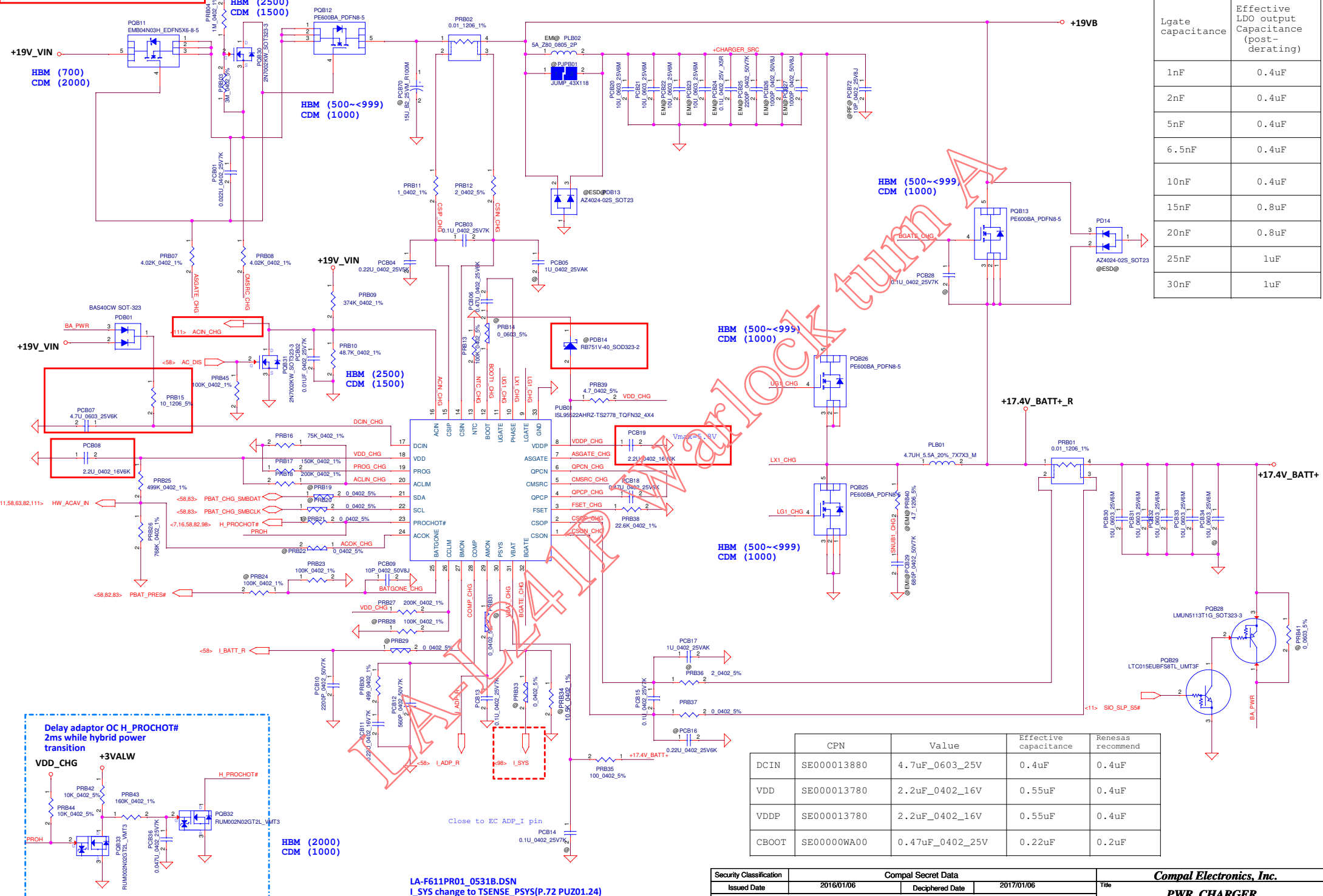
Reserve

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# Main Func = CHARGER



Lgate capacitance	Effective LDO output Capacitance (post-derating)
1nF	0.4uF
2nF	0.4uF
5nF	0.4uF
6.5nF	0.4uF
10nF	0.4uF
15nF	0.8uF
20nF	0.8uF
25nF	1uF
30nF	1uF

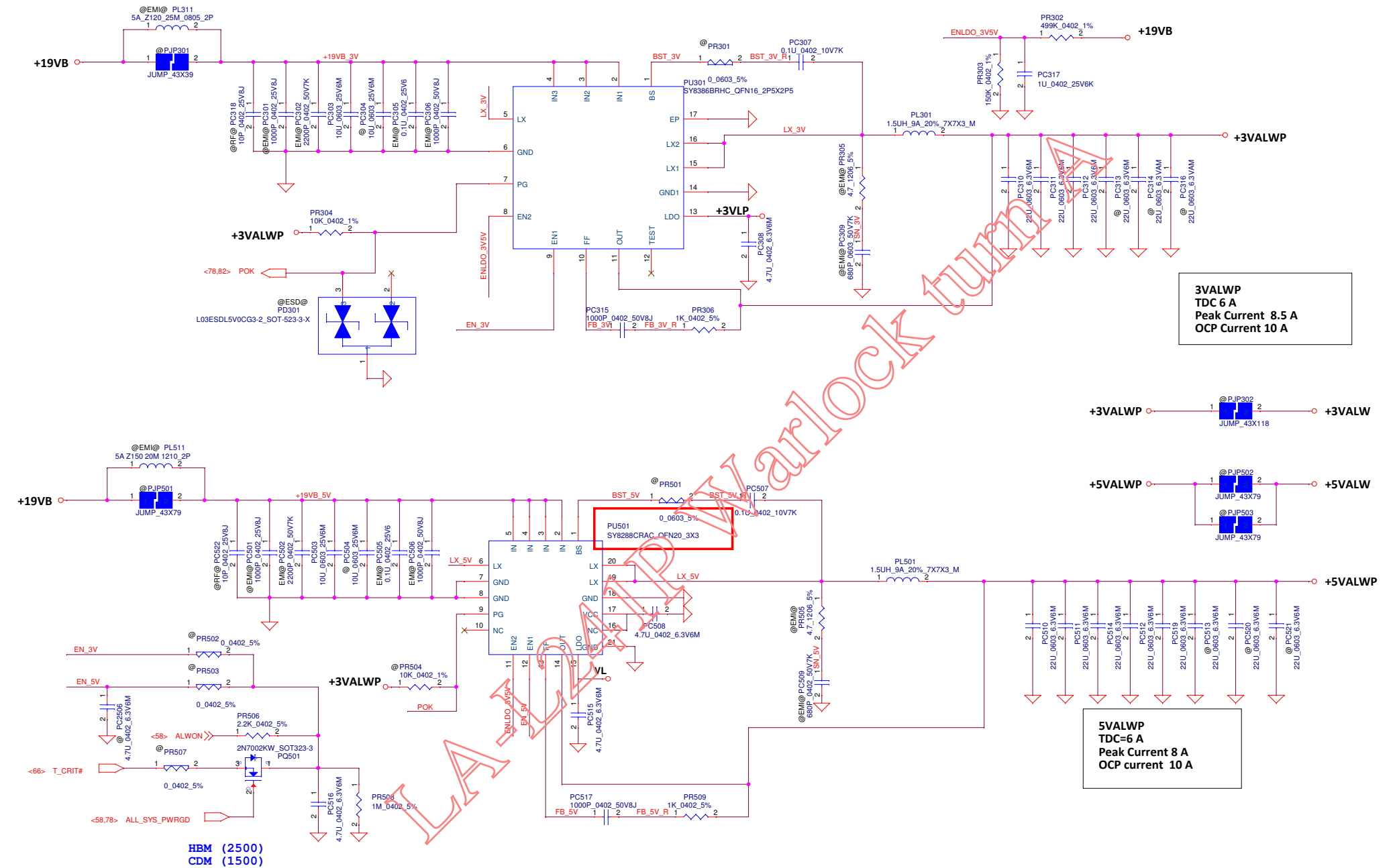
CPN	Value	Effective capacitance	Renesas recommend
DCIN	SE000013880	4.7uF_0603_25V	0.4uF
VDD	SE000013780	2.2uF_0402_16V	0.55uF
VDDP	SE000013780	2.2uF_0402_16V	0.4uF
CBOOT	SE00000WA00	0.47uF_0402_25V	0.22uF

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# Main Func = 3.3VALWP/5VALWP



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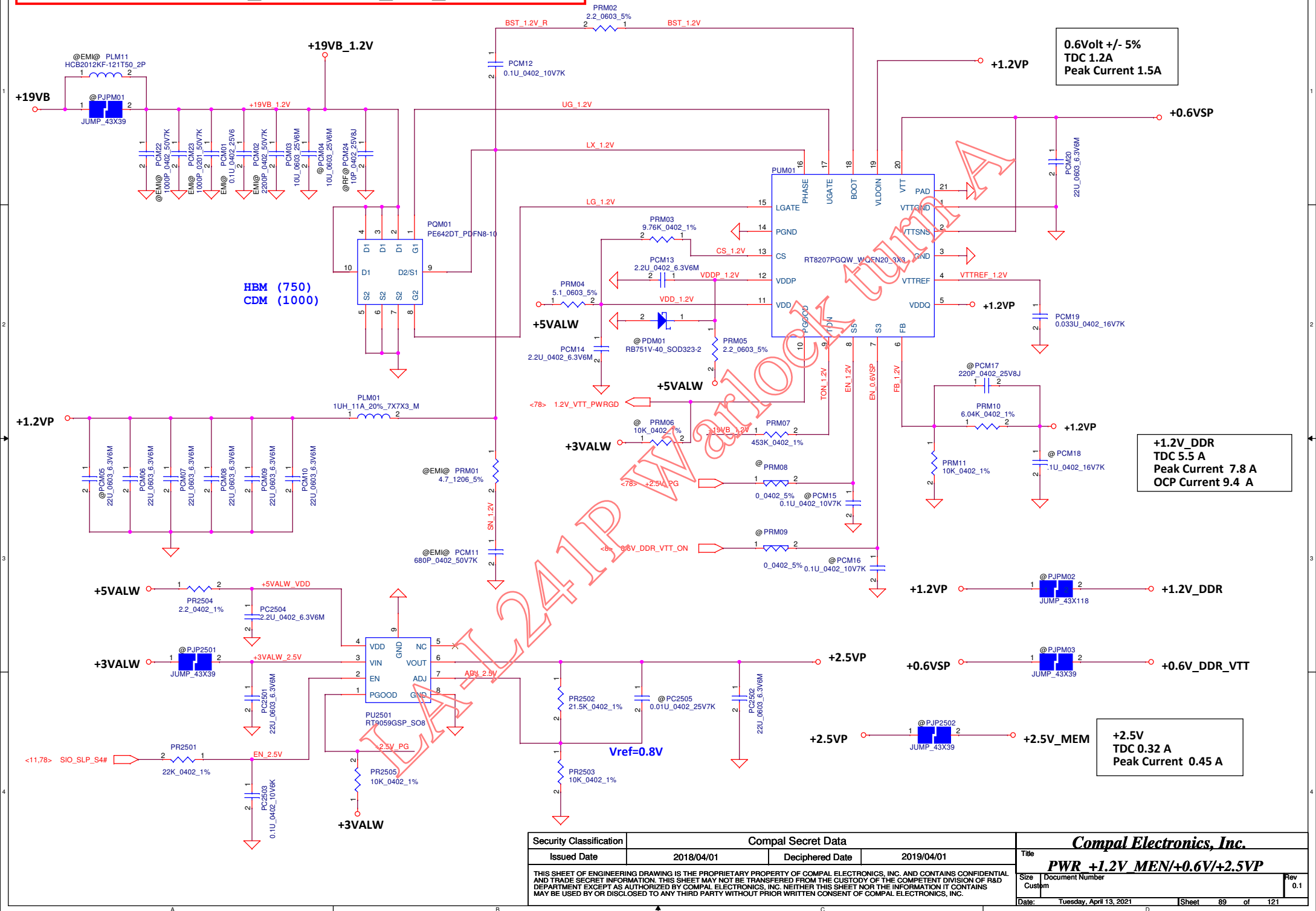
PWR 3.3VALWP/5VALWP

Reserve

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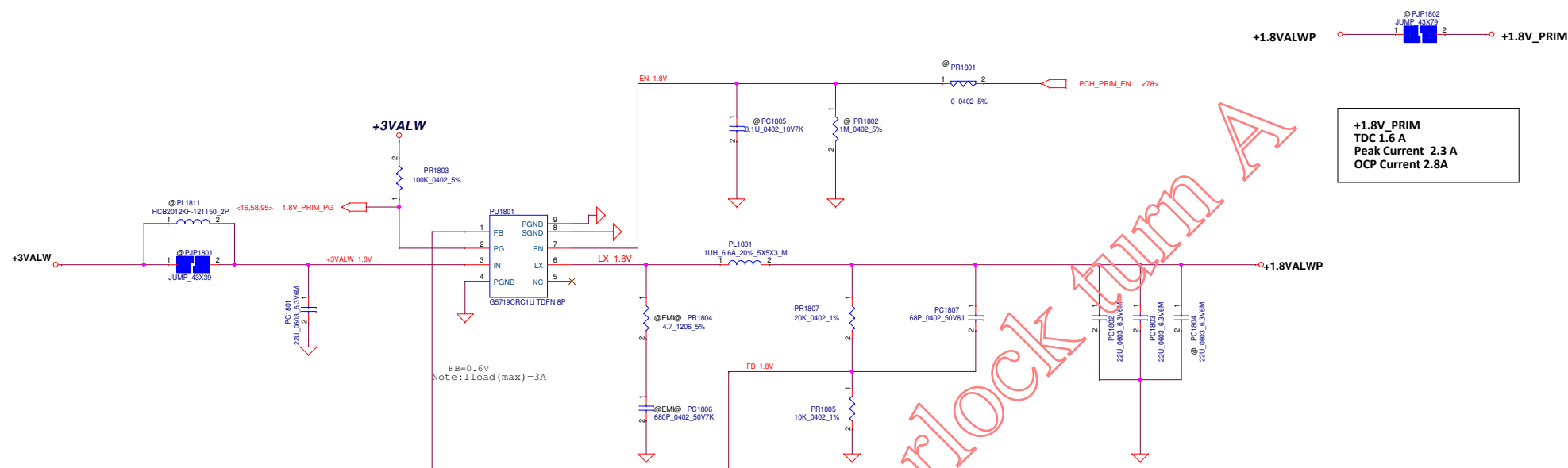
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**Main Func = +1.2V\_DDR/+0.6V\_DDR\_VTT/ +2.5VP**



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**Main Func = +1.8VALWP / +1.05VALWP**



0.0402\_5%

PR1803  
K\_0402\_5%

PU1801  
PGND 9  
SGND 8  
EN 7  
LX 6  
IN 5  
PGND 4  
NC 3  
G5719CRC1U TDFN8P

FB=0.6V  
Note: Iload(max)=3A

LX\_1.8V

PL1801  
1uH\_6.6A\_20%\_5X5X3\_M

@EMI@ PR1804  
4.7\_1206\_5%

PR1807  
20K\_0402\_1%

PC1807  
68P\_0402\_50VB

@EMI@ PC1806  
680P\_0402\_50V7K

PR1805  
10K\_0402\_1%

PR1802  
1M\_0402\_5%

PC1802  
22u\_0803\_5.3V6M

PC1803  
22u\_0803\_5.3V6M

PC1804  
22u\_0803\_5.3V6M

+1.8V

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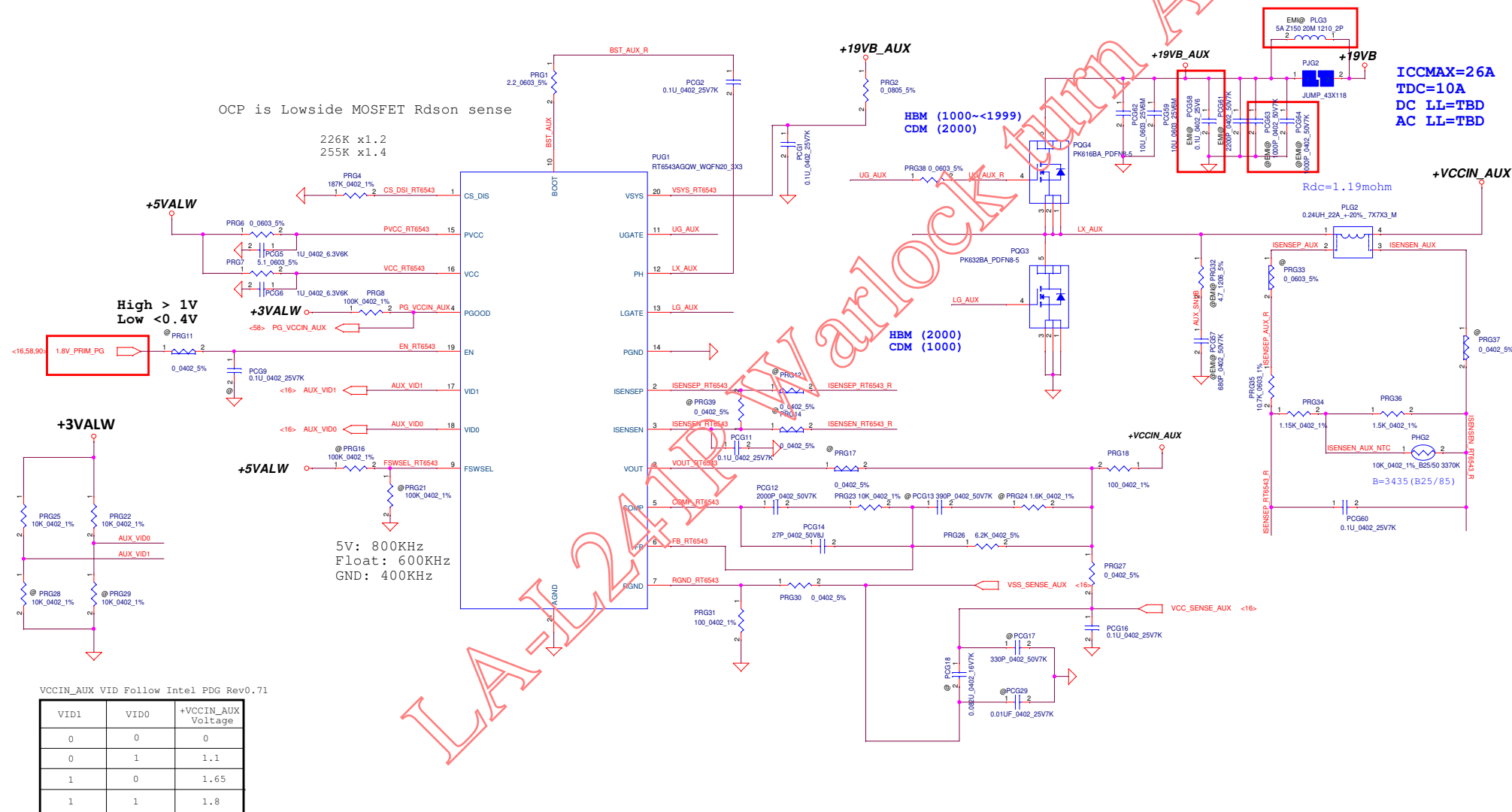
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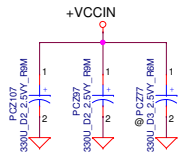
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**Main Func = VCCIN\_AUX**

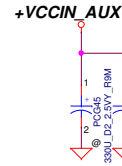
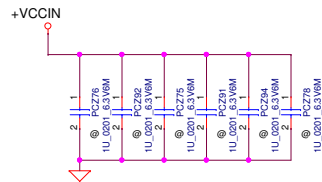
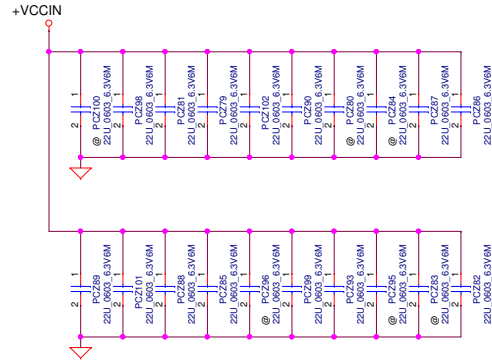


VID1	VID0	+VCCIN_AUX Voltage
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

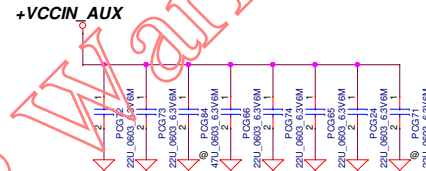
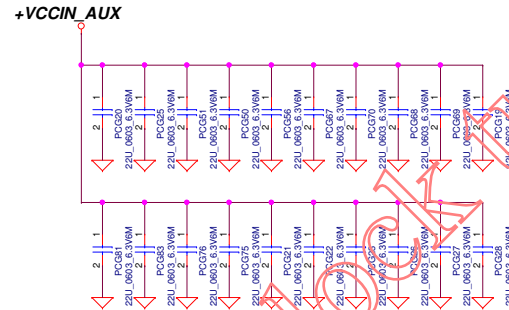
**Main Func = VCCIN/ VCCIN\_AUX**



```
Primary side :
330U_R9      *2
22U_0603     *14
```



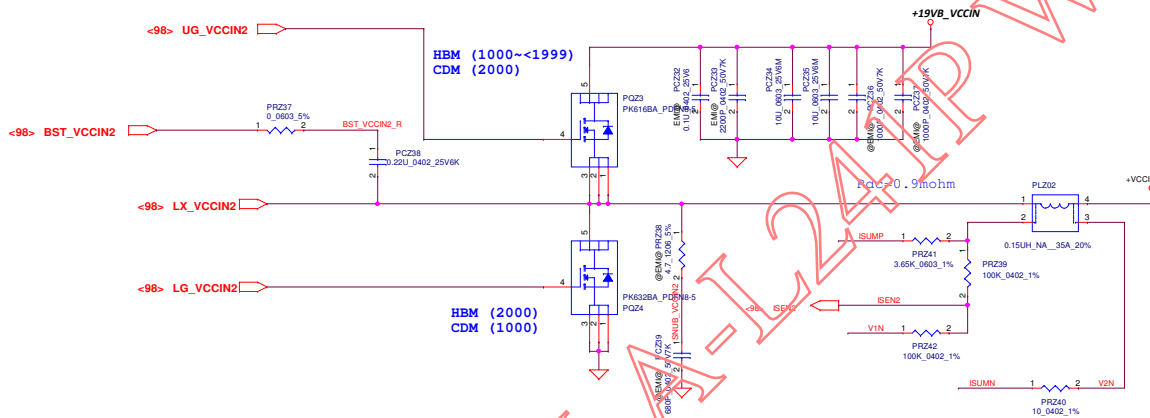
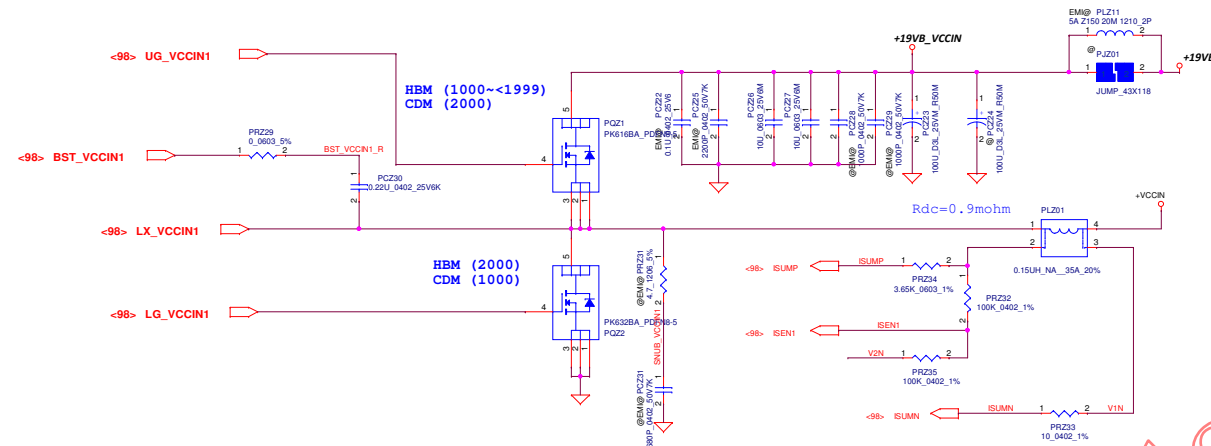
330U\_R9 \*1  
22U\_0603 \*26

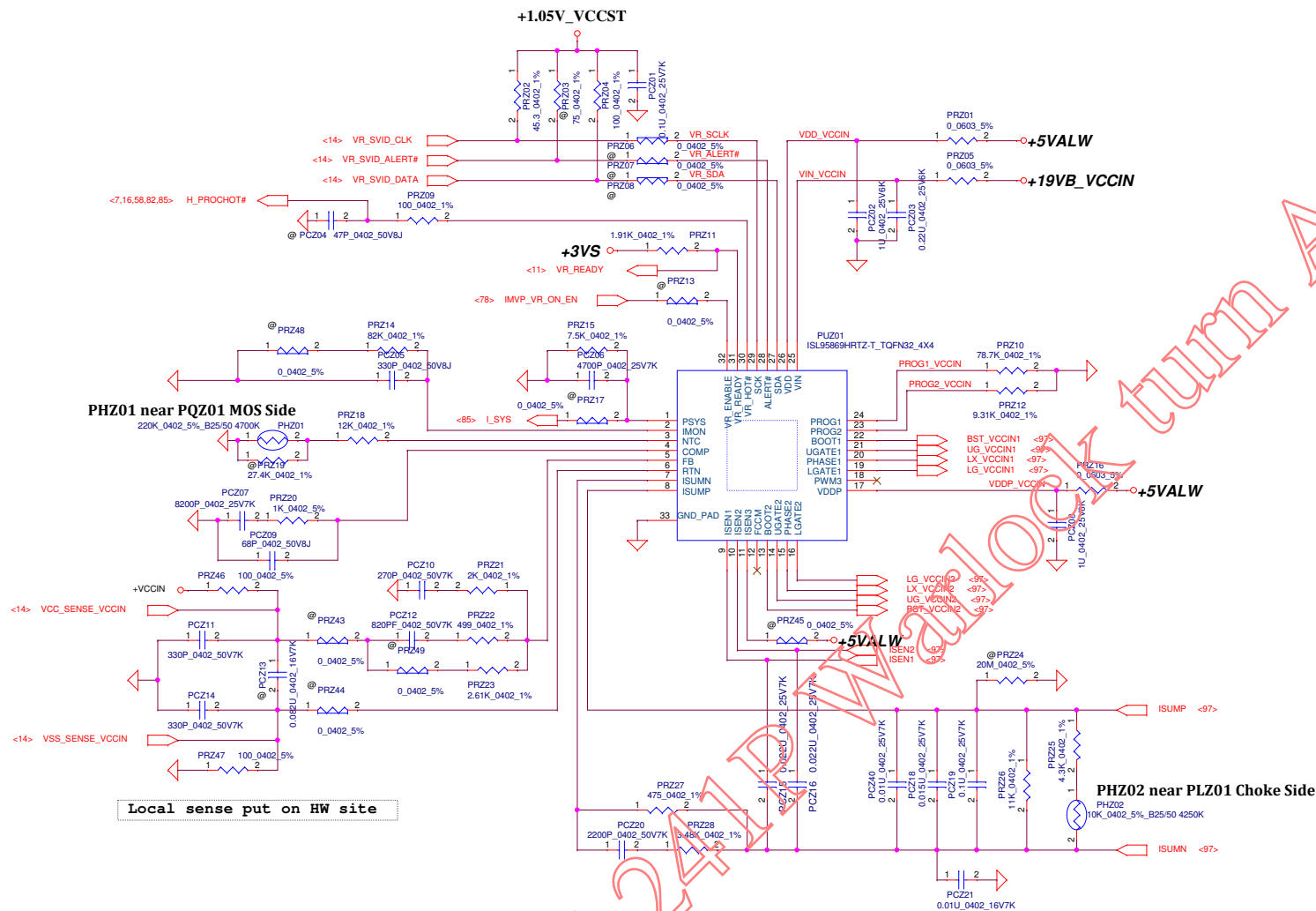


Baseline  
UP3\_4+2 15W (U42)  
ICCMAX=47A  
TDC=30A

Baseline  
UP3\_4+2 28W (U42)  
ICCMAX=55A  
TDC=36A

Frequency 750KHz





DELL CONFIDENTIAL/PROPRIETARY

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2014/11/05		2014/12/15		Document Number	
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1	P83	BATT CONN	20190423	COMPAL	RF request for RF test	Reserve PC16	0.2 (X01)
2	P84	PWR CHARGER	20190423	COMPAL	"Based on Loki G issue, change to follow Renesas recommendation "	1. PCB07 change to 0603 2. Remove PCB71 3. PRB15 change to 1206	0.2 (X01)
3	P96	NO SMOKE	20190423	COMPAL	customer request	Add page 96: reserve NO SMOKE schematic	0.2 (X01)
4	P88	PWR VCCIN	20190507	COMPAL	Change RC value for Intel EA test	"Change RC value for Intel test:  PCZ77=330UF PCZ79/80/81/82/84/85/86/87/90/96/98/99/100/102=22uF  VCCAUX Output caps 1+9 PCG46=330UF PCG19/24/28/50/51/65/71/75/76=22uF  PRZ14/25=2.21Kohm PRZ13/24=2.05kohm PRZ17/26=3.01Kohm PRZ48=37.4Kohm PRZ66=200ohm PRZ49=12.1Kohm PRZ53=14.7kohm PCZ10=82pF PCZ11=220pF "	0.2 (X01)